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Copper Wire Bonding



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Foreword

The wire bonding industry is undergoing a paradigm shift from gold to copper wire bonding—a change that is as significant as the European Union Restriction of Hazardous Substances (EU RoHS) (no-lead) mandate was to soldering. This change to copper wire bonding is driven mostly by economic considerations, and thus, the risks in the use of this technology must be carefully considered.

Since the introduction of transistors in the 1950s, interconnections between semiconductors and lead frames or substrates have been made with gold wires. At the time, gold was relatively affordable and easy to bond. While the industry did go through a period of Al-wedge bonding, gold ball bonding technology was used almost universally through the 1980s.

Due to the steep decline in the US oil imports in the 1980s, however, the price of gold rose from around US\$200 to more than US\$800 per troy ounce. As a result, the industry searched for a less expensive alternative, and copper emerged as the metal of choice. Within 3 years, most major semiconductor companies had established copper ball bonding development programs. By the early 1990s, numerous papers and patents on substituting copper for gold bonds had been published. The major advantages of copper wire bonding include having a lower, more stable cost than gold, increased stiffness (minimizing wire sweep), Al–Cu intermetallic growth rates much lower than those for Al–Au, and improved electrical conductivity. However, there were many problems with copper wire bonding, such as the hardness of copper (which can cause cratering and Al pad squeeze), ball-neck fatigue failures in plastic encapsulation during temperature cycling, oxidation of wire surfaces, decreased tail bondability, and corrosion. Furthermore, by 1998, the price of gold had declined to about US\$250/oz, and many copper wire development programs were discontinued.

Renewed interest in copper ball bonding developed around 2006 when the global recession began. Since gold has been considered a safe haven for investors in troubled times, gold prices quickly increased to US\$1,800 per troy ounce by 2012. Thus, again, economic events forced major technological changes in the wire bonding industry. A great deal of progress has been rapidly achieved in substituting copper for gold. For example, most copper wire is now coated with

Pd for better bondability. Additionally, bonding machines have been tailored for copper wire bonding. Many studies detailing new Cu bonding technology have been published, and now *this entire book is available on the bonding technology*. The success of these efforts is shown in projections that by 2015, one-third of all small-diameter wire bonds (out of the multiple trillions made) will be copper.

This book presents a comprehensive discussion of copper wire bonding, from its fundamental concepts to its use in safety-critical applications. Readers will find herein a wealth of information, including a practical how-to approach to implement this exciting new technology.

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George G. Harman
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Preface

Wire bonds form the primary interconnections between an integrated circuit chip and the metal lead frame in semiconductor packaging. Wire bonding is considered to be a more cost-effective and flexible interconnect technology than flip-chip interconnects. As of 2013, more than 90 % of semiconductor packages were interconnected by wire bonding.

Gold (Au) wire has been used for wire bonding in the electronics industry for more than 50 years because of its high tensile strength and electrical conductivity, high reliability, and ease of assembly. However, due to its high cost and continuously rising market prices, alternative wire bonding materials have been considered. Copper (Cu) is one of the most preferred alternative materials for wire bonding because of its cost advantages over Au. For example, in March 2013, the cost of Au hovered around US\$1,610/oz, compared to US\$3.45/lb of Cu. Cu wire also offers advantages in terms of higher mechanical strength, lower electrical resistance, slower intermetallic growth (with an aluminum (Al) pad), and higher thermal conductivity than Au. The higher electrical and thermal conductivity of Cu, compared to Au, enables the use of smaller diameter wire for equivalent current carrying capacity or thermal conductivity.

Replacing Au wire with Cu wire in the wire bonding process presents many challenges. Parameter adjustments for ball bond formation, stitch bond formation, and looping profile are needed. Cu is harder than both Au and Al, and therefore bonding parameters, including bonding force, must be kept under tight control. Since Cu wire is highly prone to oxidation, inert gas such as nitrogen or forming gas must be used during the bonding process. In some cases, wire manufacturers have used palladium (Pd)-coated Cu wire, which is more resistant to oxidation than bare Cu wire. Also, since bare Al pads run the risk of being damaged by Cu wires due to the high hardness of Cu and the high bonding force required, the industry has adopted Al pads that are thicker than those used in Au wire bonding, as well as pads with nickel (Ni)-based finishes.

Some semiconductor companies have adopted Cu wire bonding technology into their assembly and test sites, and are running Cu wire bonding production across a wide range of package types. For example, in May 2012, Texas Instruments shipped around 6.5 billion units with Cu wire bonding technology in its analog, embedded

processing, and wireless products. Texas Instruments also reported that all seven of its assembly and test sites are running Cu wire bonding production across a wide range of package types.

Because of the ongoing trends towards Cu wire bonding, the differences between Au and Cu wire bonding need to be understood in order to modify the manufacturing processes and reliability tests. The bonding metallurgies, process variations, and reliability of Cu and PdCu wires bonded on various surface finishes need to be evaluated. This book provides an understanding of Cu wire bonding technology, including the bonding process, bonding tools and equipment, PdCu wires, surface finishes, wire bond-pad metallurgies, wire bond evaluation techniques, and reliability tests on Cu wire-bonded parts.

The book is organized into nine chapters. Chapter 1 gives an introduction to Cu wire bonding technology. The advantages of Cu over Au, such as lower cost, higher mechanical strength, and higher electrical and thermal conductivity, are discussed. The chapter describes the adoption of Cu wire bonding in the semiconductor industry, as well as future projections for its usage.

Chapter 2 presents the wire bonding process, including the influence of process parameters on the wire bonds and bond process optimization. Bonding parameters such as ultrasonic power, ultrasonic generator current, electric flame-off current, firing time, bonding force, and temperature are discussed. The potential defects and failures that could arise during the bonding process and the bonding damage induced by tools are explained.

Chapter 3 explains the wire bonding metallurgies for Cu and PdCu wires. The most common variations are bare Cu wires, PdCu wires with Al bond pads, and Ni/Au bond pads. The interfacial metallurgies of bare Cu wire on Al-, Ni-, and Cu-based bond pads are examined. Comparisons are made between the interfacial intermetallics, Au–Al, Cu–Al, and Cu–Au, at the bond-pad interface. The growth rates and electrical, mechanical, and thermal properties of the intermetallics are presented. The bond-pad interfaces for Ni-based finishes, such as Au–AuNi, Au–AuPdNi, Cu–AuNi, and Cu–AlPdNi, are also assessed.

Chapter 4 discusses the evaluation of wire bonding performance. The criteria for good bonds are described, along with pre- and post-bonding inspection techniques. Wire bond functionality tests, such as bond accuracy tests, electrical resistance measurements, and material characterization of wire bonds are covered. Destructive and nondestructive mechanical tests, shear tests, and pull tests to evaluate the wire bond strength are discussed. The industry standards and best practices for wire bonding quality assurance and testing methods, and the common reliability tests for wire bonds, are also explained.

Chapter 5 covers the thermal reliability tests conducted on Cu wire bonds. High-temperature storage tests on Cu and PdCu wires on Al-, Au-, and Ni-based pads are discussed, and reliability test data are provided. Comparisons are made between the high-temperature storage strengths of Cu and PdCu wires. The effect of high-temperature storage on Pd distribution, as well as its effect on wire bond strength, is discussed. Cu wire bond reliability under thermal cycling and thermal shock testing is also presented.

Chapter 6 discusses the effects of high humidity and high temperature, as well as high current densities, on the reliability of Cu wire bonds. Reliability data are provided from humidity reliability tests, pressure cooker tests, and highly accelerated stress tests on Cu wire-bonded parts. Comparisons are made between the humidity-related reliability of Cu and PdCu wire bonds. Electromigration tests to evaluate the reliability of wire bonds under high electrical current are also presented.

Chapter 7 examines the pad materials and finishes for wire bonding. Cu wire bonding on Al and Cu pads is discussed. The common pad finishes, including NiAu, NiPdAu, PdAu, electroless nickel immersion gold (ENIG), electroless nickel/electroless palladium/immersion gold (ENEPIG), and electroplated silver are considered. The effect of the thickness of surface finish layers on bond strength is also explained. The chapter also discusses the effects of surface treatment on the reliability of wire bonds. The sources of contamination on bond pads, including fluorine, chlorine, carbon, oxygen, silicon, and titanium, are examined, along with their influence on wire bond reliability. The effect of lead surface contamination and pad surface roughness on wire bond strength is considered. The surface treatments, including organic coating to prevent pad oxidation and plasma cleaning to remove surface contaminants, are also explained.

Chapter 8 provides an overview of the concerns with Cu wire bonding and the industry's solutions to these concerns. Although Cu wire bonding is gaining widespread acceptance in the industry, there are a few challenges associated with it that need to be overcome. Cu wire bonding poses concerns related to Cu's hardness, propensity to oxidize, and sensitivity to corrosion, as well as the wire bonding process, bonding in specialized packages, and low yield. The industry solutions to these problems, such as the use of thicker Al pads than are used in Au wire bonding, Ni-based pad finishes, specialized capillaries, palladium-coated Cu wires, and bonding in an inert gas atmosphere, are also discussed.

Chapter 9 provides recommendations for the wire bonding process, including the use of oxidation prevention technology and bonding process parameter optimization. Recommendations for the use of PdCu wires and bond pad surface treatments, including organic coating and plasma treatments, are given. The recommended surface finishes for the pad and lead frames are listed. The microstructural characterization conducted on bond-pad interfacial intermetallics, including interfacial IMC thickness, mechanical and electrical properties of IMCs, and recommended aging temperatures for IMC characterization, is explained. Recommendations are provided for wire bond inspection and strength evaluations, reliability, qualification, and failure analysis.

Appendix A provides data on the mechanical, electrical, and thermal properties of Cu, Au, and PdCu wires. The wire bond process parameters and bond strength test data for Cu and PdCu wires for both first and second bonds are given. The reliability risk matrix for Cu and PdCu wires is provided as well. Appendix B summarizes some of the key patents in the industry, including patents for PdCu wires, Cu wire bonding methods, designs of bonding tools, underpad structures for

Cu wire bonding, and inert gas for oxidation prevention during bonding with Cu wire.

This book is intended for electronics assemblers and manufacturers transitioning to Cu wire bonding technology. It also serves as a knowledge base for readers who are interested in learning about Cu wire bonding, who will carry out evaluations of the Cu wire bonding process, and who will conduct qualification reliability tests on various packages to facilitate the mass production of semiconductor electronic products.

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Wire bonds form the primary interconnections between an integrated circuit (IC) and a metal lead frame or printed circuit board (PCB) in an IC package. Wire bonding has been widely accepted in the industry for fine pitch components with high input/output (I/O) counts. This chapter introduces copper wire bonding, its advantages over gold wire bonding, and its market adoption.

1.1 Wire Bonding Technologies

Wire bonding is an interconnection technique where two metallic materials, a wire and bond pad, are bonded using a combination of temperature, force, ultrasonic power, and time. There are three wire bonding technologies, namely, thermocompression bonding, ultrasonic bonding, and thermosonic bonding. A comparison of these three wire bonding technologies before the introduction of Cu wire bonding is shown in Table 1.1.

Thermocompression bonding utilizes temperature and pressure for bond formation. It requires a high bonding temperature (above 300 °C) and high bonding force (0.147–0.245 N) [3] which can damage the underpad structure. Ultrasonic bonding is performed by a combination of force and ultrasonic power. Thermocompression bonding utilizes high heat, while ultrasonic bonding is conducted at room temperature, thus causing less damage. Ultrasonic energy can produce morphological changes equivalent to those achieved with high heat, thus eliminating the need for high-temperature bonding. Langenecker [4] found that the elongation of a single crystal of aluminum exposed to 20 kHz vibration at a constant temperature (18 °C) was equivalent to the morphological changes accompanying heating alone. The ultrasonic energy density was $\sim 10^7$ times less than the thermal energy. For example, the morphological changes in Al occurring at a temperature of 600 °C can be achieved by the application of ultrasonic energy of 50 W/cm². Thermosonic bonding is conducted with a combination of ultrasonic energy, pressure, and heat. The bonding force and bonding time in ultrasonic bonding and thermosonic bonding are lower than those in thermocompression bonding.

Table 1.1 Wire bonding technologies [1, 2]

	Thermocompression	Thermosonic	Ultrasonic
Ultrasonic power	No	Yes	Yes
Bonding force	High	Low	Low
Temperature	High (>300 °C)	Middle (120–220 °C)	Low (room temperature)
Bonding time	Long	Short	Short
Wire material	Au	Au	Au, Al
Pad material	Au, Al	Au, Al	Au, Al
Contamination	Strongly affected	Middle	Middle

A combination of heat, pressure, and ultrasonic vibration is utilized in thermosonic bonding to form a metallurgical bond between two materials. During thermosonic bonding, the bonding wire is softened by adjusting the power and duration of the ultrasonics. Heat is applied by placing the packaged on a heated stage. Sometimes, a heated bonding tool is also used. The bonding force is applied by pressing the bonding tool into the wire to force it into contact with the bond pad surface. The amount of weight applied to the bonding wire to establish mechanical contact between the bonding wire and the bonding pad surface is controlled by the tool force. Ultrasonic energy is applied by vibrating the bonding tool while it is in contact with the wire. Heat and ultrasonic energy soften the wire and pad metallization, and the bonding wire is deformed with the bonding tool against the pad metallization, forming a metallurgical bond.

1.2 Ball Bonding vs. Wedge Bonding

Wire bonds can be classified into two types: ball–wedge bonding and wedge–wedge bonding. The majority of wire bonds in electrical packages are formed with ball–wedge bonds since ball–wedge bonding is much faster than wedge–wedge bonding [2]. However, wedge bonding is preferred in deep access, fine pitch, and low- and short-loop applications, including microwaves and optoelectronics. Ball bonding requires three axes of movements (X -, Y - and Z -direction), whereas wedge bonding requires four axes of movement (X -, Y -, and Z -direction, as well as θ). Ball–wedge bonding commonly uses gold and copper wires, whereas wedge–wedge bonding uses aluminum wires. A comparison of ball bonding and wedge bonding is shown in Table 1.2.

Among the wire bonding technologies, thermosonic bonding is the most common wire bonding technique used in semiconductor packages. Also, ball–wedge bonding is more commonly used than wedge–wedge wire bonds. This book henceforth focuses on the thermosonic wire bonding technique, and ball–wedge wire bonds. Thermosonic bonding forms the first bond, or the ball bond (normally on the chip pad), and then the second bond, or stitch bond (also called the wedge bond), to another metal (usually on a substrate). Before the first bond is formed, the free end of the wire is divided into three parts: a free air ball (FAB), a heat-affected zone (HAZ),

Table 1.2 Comparison of ball bonding and wedge bonding applications [1]

	Ball bonding	Wedge bonding
Bonding techniques	Thermocompression (T/C) Thermosonic (T/S)	Thermosonic (T/S) Ultrasonic (U/S)
Temperature	T/C—> 300 °C T/S—120–220 °C	Al wire—U/S at room temperature Au wire—T/S 120–220 °C
Wire size	Small (<75 μm)	Any size wire or ribbon
Pad size	Large (3–5 times of wire diameter)	Smaller pad size than a ball bond. Good for the microwave application. The pad size = 2–3 times of wire diameter (could be = 1.2 times of ribbon width)
Pad material	Au, Al	Au, Al
Wire material	Au	Au, Al
Speed	Fast (10 wires/s)	Relatively slow (4 wires/s)

and as-drawn wire due to the effect of electrical flame-off (EFO). FAB formation is achieved by ionization of the air gap by the EFO process. A schematic representation of the wire bonding cycle is shown in Fig. 1.1. During steps 1 and 2, the bonding tool (called a capillary) travels down to the first bond location (bond pad). The first bond (ball bond) is made in step 3 by bonding a spherical ball to the pad using thermal and ultrasonic energy. Looping motions are programmed to obtain the desired loop height and shape (steps 4, 5, and 6). The second bond (stitch/wedge bond) bonds the opposite end of the wire loop to the metal of the substrate (step 7). After the bonding tool (capillary) rises to pay out the wire tail, the tail is broken off and the bonding tool rises up further to the ball formation height (steps 8, 9, and 10).

The bonding process governs the quality of the formed wire bonds. Table 1.3 lists the factors in the bonding process that affect the wire bond quality. These factors can be summarized as the accuracy of the bond wire placement; the form of the bond; the physical parameters of the bonding process; the wire metallurgy; the materials, morphology, and surface cleanliness of the bond pad metallization; and any degradation of the wire and bond pad [5].

1.3 From Gold to Cu Wire Bonding

Gold (Au) wire has been the most common wire used to interconnect aluminum (Al) pads on IC chips to lead frames, and it has been considered acceptable in terms of manufacturing and reliability. However, copper wire is less expensive than gold. This has driven the transition to copper wire [6]. Figure 1.2 shows the price of gold from 2008 to 2013. It can be seen that gold prices rose considerably in those 5 years, leading to an exploration of alternative wire metallurgies [7, 8].

The most common alternative wire materials include silver and copper. Table 1.4 shows a comparison of the properties of Au, Cu, and Ag wires. As seen in Table 1.4,

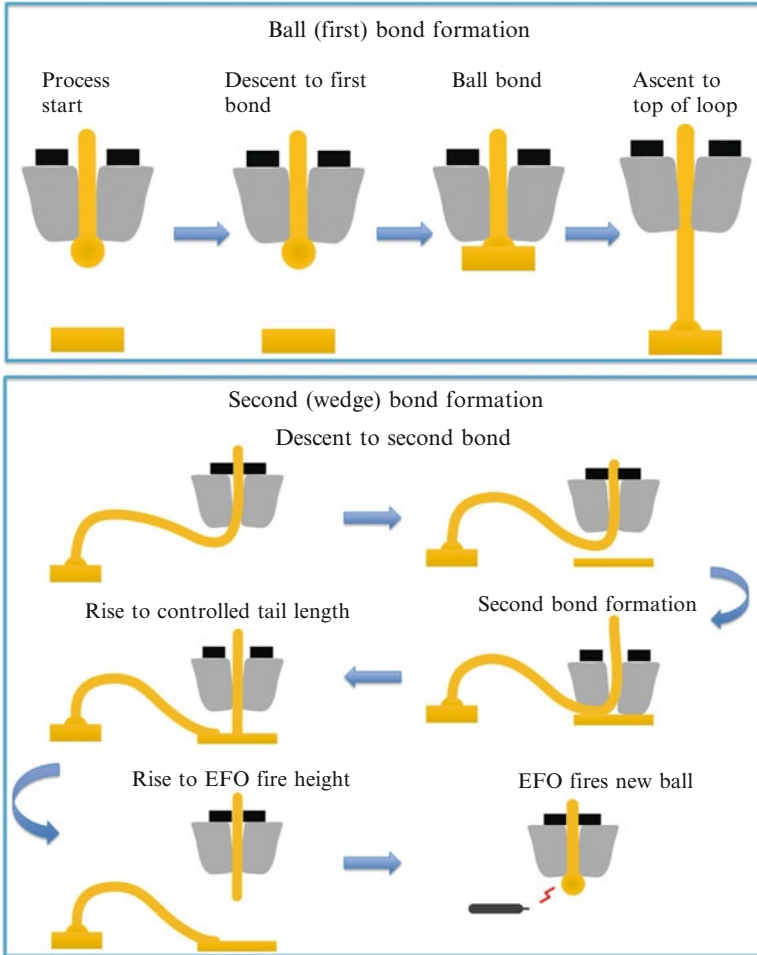


Fig. 1.1 The ball-wedge wire bonding cycle

Cu has higher hardness and Young's modulus as well as higher thermal and electrical conductivity than Au.

The comparison of Cu and Ag wires in Table 1.4 shows that Ag has lower Young's modulus and lower hardness than Cu. Hence, Ag wire could be bonded with lower bonding force than required for Cu, with less potential damage to the underlying circuitry. Also, the cost of Ag is about 5 % of the cost of Au as of March 2013, so there is a cost advantage for Ag as well. However, Ag wire bonding has reliability concerns [11, 12]. Yoo et al. [12] reported that Ag wire on Al pads has reliability concerns under high-temperature storage (HTS) tests (175 °C) and showed

Table 1.3 Factors affecting bond quality [5]

Materials	Wire	Wire material
		Alloying
		Purity
		Additives
		Diameter
		As-drawn vs. annealed
		Hardness
		Ultimate tensile strength
		Percent elongation
		Lot-to-lot variation
	Bonded surface	Storage conditions
		Cleanliness
		Pre-cleaning methods: Plasma
		Freedom from defects
		Surface condition
Capillary or wedge	Force applied	
		Ultrasonic
		Frequency
		Power
		Resonant system
	Time	
	Tool	Size and shape
		Material: Trend to ceramic
		Surface finish
		Cleanliness
		Wear
Machine	Stage temperature	150–200 °C is typical for thermosonic bonding
	Bond positioning	Pattern recognition
	Wire loop	Bond geometry
		Takeoff angle
		Loop height
	Freedom from vibration	
	Rigidity	

interfacial cracking after 300 h. Pure Ag wire poses the concerns of silver migration and corrosion, and it requires nitrogen cover gas for bonding. Alloyed silver wires are being considered [13], such as Ag wire alloyed with Au and Pd. With the addition of Au and Pd, the cost of alloyed Ag wire increases. The cost of alloyed Ag wire is less than the cost of Au but more than the cost of palladium-coated Cu wire. However, with the addition of other elements to the Ag, the electrical resistance increases, which is undesirable for many applications. Also, Ag alloy is not suitable for all applications; for example, Ag is not suitable for use in radio-frequency applications [8].

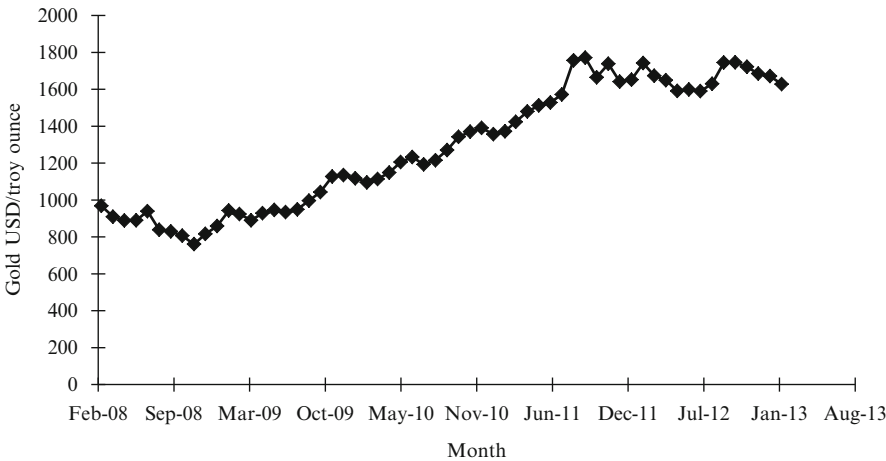


Fig. 1.2 Au prices from 2008 to 2013 [9]

Table 1.4 Material properties of Au, Cu, and Ag wires [10]

Property	Au	Cu	Ag
Thermal conductivity (W/mK)	320	400	430
Electrical resistivity (Ω m)	2.20	1.72	1.63
Young’s modulus (GPa)	60	130	82.50
Poisson’s ratio	0.44	0.34	0.364
Yield stress (MPa)	32.70	200	45.50
Coefficient of thermal expansion (ppm/ $^{\circ}$ C)	14.40	16.50	18.90
Vicker’s hardness (MPa)	216	369	251

In light of the concerns with the forms of wire bonding described above, copper wire bonding has been widely accepted as an alternative to gold wire. Figure 1.3 shows the 5-year (2008–2013) trend in the price of copper.

Along with being relatively inexpensive, copper provides high electrical and thermal conductivity. Bare Cu and palladium (Pd)-coated Cu wires are the two forms of Cu wire in use in the industry. A comparison of the mechanical properties of wire metallurgies reveals that both PdCu and bare Cu wires are harder than Au wire, which provides a higher tensile strength (see Table A.1). Other desirable mechanical properties for Cu wire and PdCu wire over Au wire are low electrical resistance and higher thermal conduction.

Copper wire has higher mechanical strength, lower yield strength [15], higher electrical conductivity ($5.88 \times 10^7 \Omega$ m vs. $4.55 \times 10^7 \Omega$ m) [16–18], slower intermetallic compound (IMC) growth (with an Al pad) [16–20], and higher thermal conductivity (394 W/m K vs. 311 W/m K) [21] than conventional gold wire. The better electrical and thermal conductivity of copper enables the use of smaller diameter wire for equivalent current carrying or thermal conductivity.

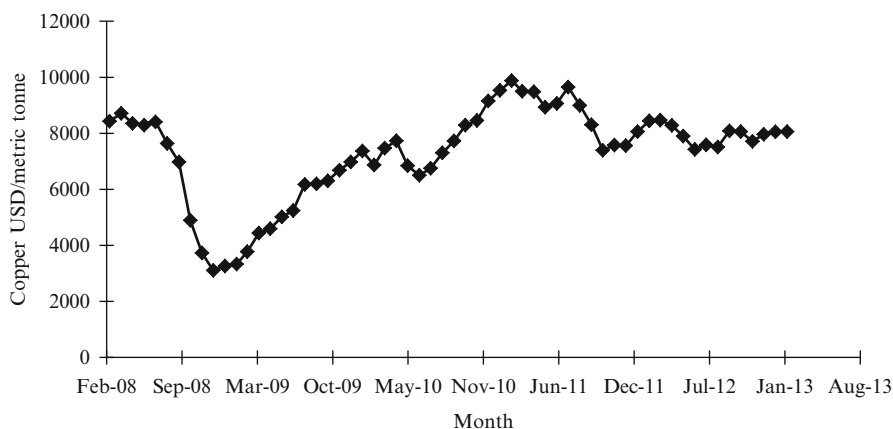


Fig. 1.3 Cu prices from 2008 to 2013 [14]

This makes copper wire a better option for high-power applications. The lower IMC thickness at a Cu–Al interface leads to lower heat generation, lower electrical contact resistance ($7.0\text{--}8.0 \times 10^{-6} \Omega \text{ cm}$ vs. $37.5 \times 10^{-6} \Omega \text{ cm}$) [22], and better reliability than at an Au–Al interface.

Since copper wires conduct heat faster than gold, they allow for a shorter HAZ. As very high currents and temperatures are reached during EFO firing, the heat generated during FAB formation will promote grain growth along the wire, which is undesirable for wire bond reliability [23]. Better thermal conductivity can reduce grain growth and shorten the HAZ, resulting in improved looping performance, especially in ultralow-loop applications that demand stricter requirements at the wire neck area [24].

Investigations of the annealing effect on copper wire mechanical properties have revealed that with temperatures greater than 200°C , copper wire has a fully annealed structure, its tensile strength and hardness decrease, and its elongation increases [25, 26]. After EFO firing, the FAB microstructures of the copper wire consist of column-like grains that grow from the HAZ to the Cu ball. The decreased hardness and strength of the HAZ result in breakage sites of the wires in the HAZ near the Cu balls.

Copper also has a higher tensile strength and is stiffer and harder than gold, resulting in higher shear strength [27–29] and pull strength [30]. Cu has been reported to have better wire sweep performance than Au during molding and encapsulation of fine-pitch devices [15]. Teh et al. [31] reported the wire sweep performance of copper to be dependent on the fabrication processes and heat treatments, as well as on the wire location during the transfer molding process.

Cu achieves longer/lower loop profiles and provides better looping control than Au, including less wire sagging [32]. Copper wire bonding allows longer wire lengths and smaller wire diameters in the same package, thereby providing more flexibility in the wire bonding process than is seen with Au bonding.

1.4 Market Adoption

The semiconductor industry has seen an increase in the use of copper for wire bonding applications. Kulicke and Soffa (K&S) reported that by the end of 2010, the installed base of copper wire capable bonders rose to 25 %, up from less than 5 % in the beginning of 2009 [33]. The installed base is a measure of the number of units of a system in use. As seen in Fig. 1.4, a 5-year projection of the installed base of bonding machines shows that the installed base for copper wire bonding machines will rise steadily up through 2015.

Several semiconductor companies, including Amkor and Texas Instruments (TI), have adopted copper wire bonding technology in their assembly lines [35]. TI announced in May 2012 that it shipped around 6.5 billion units of copper wire bonding technology in its analog, embedded processing, and wireless products. TI also reported that all seven of its assembly and test sites are running copper wire bonding production across a wide range of package types, including quad flat no lead (QFN) packages, ball grid array (BGA) packages such as new fine-pitch ball grid array (nFBGA) and plastic ball grid array (PBGA), package-on-packages (PoPs), quad flat packages (QFPs), thin quad flat packages (TQFPs), thin shrink small outline packages (TSSOPs), small outline integrated circuit (SOIC) packages, and plastic dual-inline packages (PDIPs) [36]. Altera has projected that by 2015 all wire bond packages will be converted from gold to copper wire. Advanced Semiconductor Engineering (ASE) reported that the sales of copper bonding grew to 39 % (US\$325 million) in the second quarter of 2012, up from 24 % in the first quarter of 2011. Siliconware Precision Industries (SPIL) reported that sales generated from copper wire bonding accounted for 53 % of the company’s overall wire bonding revenues in the second quarter of 2012, which was up from 50 % at the end of 2011 and 30 % at the end of second quarter of 2011 [37, 38]. This number climbed to 55 % in the third quarter of 2011, and to 63 % by the end of 2012 [39].

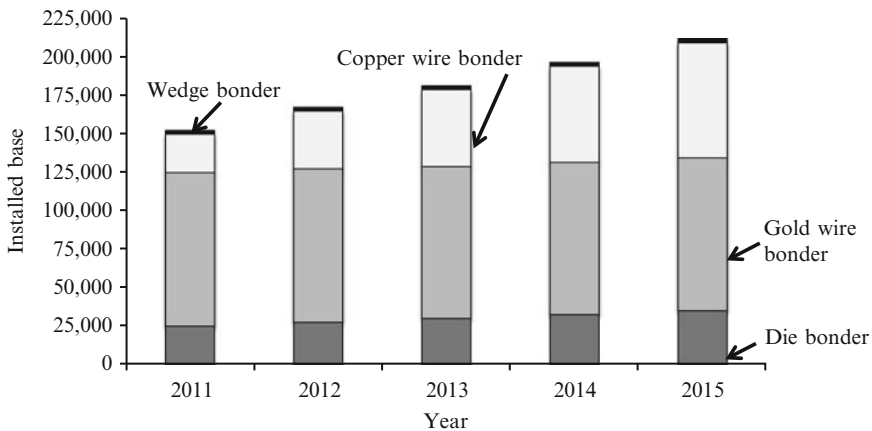


Fig. 1.4 Installed base of copper and die bonding machines for 2011–2015 [34]

It was recently reported that Cu wire bonding will account for 65 % of SPIL's overall wire bonding sales in the first quarter of 2013, and is expected to climb to 70–80 % by the end of 2013 [40].

Heraeus, Amkor, Altera, Carsem, Freescale, Infineon, and several Japanese companies have also undertaken Cu wire bond projects at their respective facilities. Other companies are considering the adoption of Cu wire bonding and are assessing the total cost of the conversion to Cu. Companies are developing Cu wire bonding for 45 μm pitch, low- k and extra-low- k (ELK) device dielectrics, and optoelectronics and LEDs. The conversion to Cu wire for 3-D packaging and stacked dies has also been investigated and is ready for production [41].

1.5 Summary

This chapter discusses the common wire bonding technologies in the industry, namely, thermocompression, ultrasonic, and thermosonic wire bonding. Thermosonic wire bonding is the most common wire bonding technique used in the industry. The thermosonic wire bonding process is explained, and factors affecting the bond quality are discussed.

The electronics industry is moving away from Au wire bonding due to the rising prices of Au. The industry is considering other lower cost alternatives to Au, the most popular being Ag wire (both pure and alloyed) and Cu wire. Although Ag wire offers cost advantages compared to Au and has better electrical conductivity than Cu, pure Ag has reliability concerns. These reliability concerns can be overcome by using alloyed Ag wire, but this increases the electrical resistance of the wire as well as the cost.

Cu wire is the most suitable alternative to Au because of cost considerations as well as better electrical and mechanical properties and the better interfacial reliability of Cu than Au wire. Copper offers higher electrical and thermal conductivity and better HTS performance than gold. Other advantages include a shorter HAZ and higher tensile strength, stiffness, and hardness than gold.

Many semiconductor companies, such as Texas Instruments, ASE, and SPIL, are adopting copper wire bonding technology into their assembly and test sites and are running copper wire bonding production across a wide range of package types.

In this chapter, the details of the wire bonding process are discussed. The bonding wire configurations used in the electronics industry are listed, and wire parameters such as wire processing, wire purity, and wire diameter are explained. Since the use of bare copper wires is a concern owing to the propensity of copper to oxidize, oxidation prevention technology is needed. The chapter discusses the two oxidation prevention technologies used in the industry, including cover gas and oxidation prevention coating. The wire bonding parameters govern the quality of formed free air balls (FABs) and subsequent first and second bonds. The effect of electrical flame-off current and firing time on formed FABs, and the effect of ultrasonic energy, bonding force, bonding temperature, and time on wire bond quality, is explained, and the optimal parameter ranges are listed. The bonding tools for copper wire bonding are explained and the failures resulting from improper bonding are also listed.

2.1 Bond Wire

Wire purity and the processing undergone by the wire during wire drawing operation determine the mechanical properties of the bonding wire. The mechanical properties relevant for wire bonding are elongation percentage and the breaking strength. Additionally, the stress state of the wire—residual stress or stress free (fully annealed)—determines the looping characteristics of the wire. The use of annealed wire reduces the variation in the bond strength and makes the bonding process less sensitive to thermal effects. A high-purity wire is desired, which is melted in a high vacuum to obtain a homogeneous microstructure. The resulting cast bar is subjected to multiple stages of drawing through a series of dies to reduce the wire diameter for bonding. The thinner the wire requirement, the more stages of wire drawing the wire undergoes. Wire processing should ensure that the wire has a clean surface and smooth finish so that it easily comes out of the spool without

snagging [5]. Bare Cu wires of varying purity (3–6 N) are used in the industry, and the wire cost is directly proportional to the wire purity. Also, as the wire purity increases, the wire becomes softer.¹

Bond wire manufacturers often dope pure Cu wire with additives to enhance the wire bondability and minimize the Al splash. For the same wire thickness, a Cu FAB is larger in diameter than the corresponding Au wire. Hence, to achieve the same FAB diameter, Cu wires are 2.54 μm thinner than Au wire. Bare Cu wires used in the industry have purities of 3–6 N, with 4 N as the most commonly used [42, 43]. Srikanth et al. [44] investigated Cu wires of varying purity, including 3, 4, and 5 N, and 50 μm thickness. They reported that higher purity wires have lower flow stress than lower purity wires (95.5 MPa for 5 N, 115 MPa for 4 N, and 120 MPa for 3 N), since they have fewer grains. Cu wire of 3 N purity had fine columnar grains in the initial state, as well as after melting (FAB formation). On the other hand, wires of 4 and 5 N purity had large grain sizes and few columnar grains in both the initial state and after melting. The grain direction on the FAB affects the hardness and elastic modulus of the FAB, wherein the lack of directionality results in softer wires. The low flow stress in 5 N wires was attributed to the lack of directionality in the grains. Because of the lower flow stress, a lower bonding force is required, which results in a lower Al splash. The high-purity wires showed high twinning features, which can impair the deformation processes during the bonding operation. On the other hand, for 3 and 4 N FABs, the number of grains in the [100] direction was larger than that in the [110] and [111] directions [44]. The thermomechanical processing that the wire undergoes determines the residual stress states in the wire and the mechanical properties, including the hardness and tensile strength. The grain structure of the wire can be optimized for the individual purity level by the wire processing steps, including the deformation and annealing steps during wire drawing. Optimization of wire purity and microstructure can help achieve the desired mechanical properties, such as wire elongation and tensile strength. Wires with a high elongation strength have smaller grains and higher tensile strength [45].

Another consideration for the bonding wire is the wire diameter. The choice of wire diameter depends on the compatibility with the process and the required current carrying capacity. For consumer electronics, the common wire diameter range is 18–25 μm , whereas for the power electronics, the common wire diameter range is 20–50 μm [46].

The use of bare Cu is a concern due to the propensity of Cu to readily oxidize. The use of oxidation-resistant coatings is one way to address the problem of Cu oxidation. Al-coated Cu wires for room-temperature wedge–wedge bonding have been shown to suppress oxidation and have better pull strength, better metallic contact formation, and better storage capabilities than bare Cu wires [47]. Al-coated wire is suited for room-temperature bonding on low-temperature co-fired ceramics

¹ The material purity in % or Nines scale is denoted in terms of purity in parts-per-million (ppm). For example, 1 N = 90 %, 2 N = 99 %, 3 N = 99.9 % and so on.

Table 2.1 Bonding wire comparison: Au, Cu, and PdCu [54]

	Au	Cu	PdCu
Cost	High	Low	Low (higher than Cu)
Cover gas	No need	Forming gas	Forming gas or N ₂
FAB hardness	Compatible to Al	~40 % harder than Au	~10 % harder than Cu
First bond process	Good process window	Narrower than Au	Same or slightly narrower than Cu
Second bond process	Same	Same	Same
Portability requirement	Moderate	High	High
Reliability	Good	Good; more stringent mold compound than that for Au	Same or slightly better than Cu

with silver and gold metallization. Among the oxidation prevention coatings (Au, Ag, Pd, and Ni), Pd coating on Cu has shown sufficient potential to replace Au wire due to its excellent bondability and reliability at a relatively low cost [48–53]. Pd is a semi-noble metal with similarities to both Ag and Pt. PdCu is oxidation free, and Pd has good adhesion to Cu wire and higher tensile strength than bare Cu wire when bonded on Al pads. Table 2.1 shows a comparison of Au, Cu, and PdCu wires.

Because of the Pd layer on Cu wire, there is always a layer of Pd or a Pd-rich phase that protects the bonded ball from an attack of corrosion. Easing the use of Pd may also ease the stringent molding compound requirement. Pd prevents the formation of CuO and can form a bond with N₂ without requiring forming gas. Figure (2.1a, b) shows a comparison of Cu and PdCu wires bonded on Al. This comparison of the first bonds of PdCu and Cu wires shows that PdCu-bonded ball has lower Al pad splash than Cu-bonded ball.

Robustness in the second bond is the most important reason to adopt PdCu wires [52, 55]. This robustness has led to an improved C_{pk} (process capability index). The stitch pull strength of PdCu wire is more than 50 % higher than bare Cu [51]. PdCu wire on an aluminum bond pad has also been demonstrated to perform better than bare Cu in high-humidity conditions, such as in the highly accelerated stress test (HAST), pressure cooker test (PCT) [50], temperature cycling test (TCT), and high-temperature storage (HTS) test. Table 2.2 shows a bond strength and defective second bond ratio comparison of Au, Cu, and PdCu wires. The PdCu wires have a higher second bond strength than bare Cu wires and zero defective second bonds [48]. PdCu also works better at higher ultrasonic generator (USG) current levels than Cu wire. It should be noted, however, that due to the higher hardness and rigidity of PdCu over Cu, a higher bonding force is needed for PdCu wires, which could increase the risk of Al splash and pad damage [56]. Hence, careful optimization of bonding parameters is needed for PdCu wires.

Since PdCu wire has a larger diameter than bare Cu wire, the FAB diameter for PdCu wire needs to be smaller than for bare Cu wire. Because of the Pd layer on the Cu wire there is always a layer of Pd or a Pd-rich phase that protects the bonded ball from an attack of corrosion. Easing the use of Pd may also ease the stringent molding compound requirement. Pd prevents the formation of CuO and can form

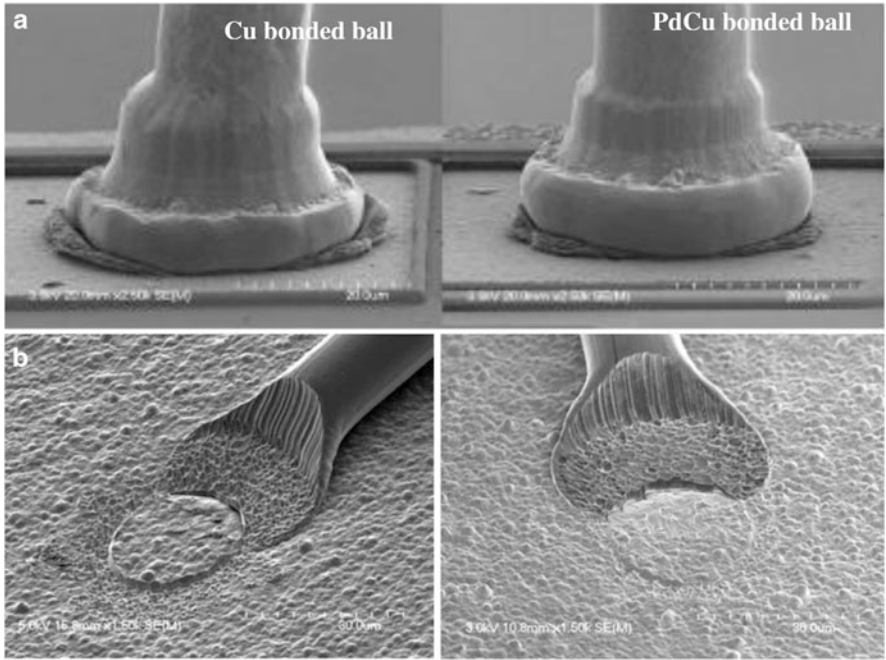


Fig. 2.1 Cu and PdCu wires: Comparison of (a) first and (b) second bonds in [51]

Table 2.2 Bond strength and defective second bond ratio comparison [48]

	Au	Cu	PdCu
First bond strength (N)	0.256	0.215	0.352
Second bond strength (N)	0.053	0.026	0.074
Defective second bond ratio (ppm)	0	7933	0

a bond with N_2 without requiring forming gas. A comparison of N_2 and forming gas for PdCu wire (15 μm) showed that forming gas is superior to N_2 since it is not sensitive to changes in electrical flame-off (EFO) (FAB diameter relative standard deviation: 0.94; ball-to-wire offset: 0.53 μm) [57]. Comparisons of bare Cu and PdCu wire have shown that at a higher EFO current, an FAB with bare Cu wire has higher hardness caused by having smaller grains. Varying the EFO current in PdCu wire causes the hardness of the wire to vary due to the different distributions of the PdCu alloy in the FAB [58].

Although Pd coating prevents the oxidation of Cu, it introduces new challenges for wire bonding. It is 2.5 times more expensive than bare Cu [59] and has a higher melting point than Cu [59]. The industry is thus looking to optimize Pd thickness to reduce costs, decreasing the Pd thickness from 0.2 to 0.1 μm [54]. PdCu is harder than pure Cu and, hence, increases the risk of pad cracking and damage to the circuitry under pad (CUP). The Pd distribution can also affect the reliability of Cu wire-bonded devices, but as of 2013 there was no method to control Pd distribution.

2.2 Oxidation Prevention Technology

FAB formation requires the generation of high voltage across the EFO gap, causing a high current spark to discharge and melt the tail of the Cu wire to form a spherical ball. Oxidation must be avoided in order to obtain a symmetrical FAB without deviation in size [60]. Cu oxidation during ball formation inhibits the formation of a spherical ball, which in turn affects the reliability of the first bond. Under high-temperature and high-humidity environments, copper oxidation at the interface of the Cu–Al bonding region causes cracks and weakens the Cu–Al bonding. Copper oxidation typically starts at the wire region and then spreads to the upper bonded area and then to the bonding interface with time. Cu oxidation also causes corrosion cracks.

Since Cu oxidizes quickly, Cu FABs need to be formed in an inert gas environment. Oxidation can also occur if the cover (inert) gas flow rate is not sufficiently high to provide an inert atmosphere for the FAB formation [61]. It has been reported that the use of single-crystal Cu wires eliminates the need for cover gas during bonding [62]. Requiring inert gas, such as forming gas, to address the oxidation problem adds complications to the bonding process and results in a narrow process window.

The oxidation of Cu is prevented in two ways: use of an inert gas (nitrogen or forming gas) during bonding, and use of oxidation prevention coating on the Cu wire [42, 63, 64]. The use of N₂ as the cover/shielding gas has resulted in defective FABs. Since forming gas contains 5 % H₂ (95 % N₂, 5 % H₂), it has better anti-oxidation properties than N₂ and is the cover gas for Cu wire bonding. The main purpose of injecting forming gas (FG) is to form an inert gas shroud around the copper tail and the FAB to prevent oxidation prior to bonding. The use of H₂ has the twofold purpose of helping to melt the Cu, as well as acting as a reducing agent to reduce the copper oxide back to Cu [60].

2.3 Free Air Ball Formation

FAB formation starts with the Cu wire being heated and subsequently melted by the low-energy plasma discharged. The molten wire turns into a spherical ball under the effect of surface tension. At the end of discharge, the molten spherical ball starts cooling and then solidifies to form a FAB [65]. Qin et al. [66] compared Au and Cu balls on Al pads and found that non-optimized bonding conditions resulted in over-bonded balls for Au wire and under-bonded balls for Cu wire. Although Cu wire bonds showed higher pull strength than Au wire bonds, Cu wire bonds had a larger standard deviation, which indicates that more process development is required to optimize the process conditions for Cu wire bonding. Figure 2.2(a, b) shows the FAB micrographs for Au and Cu wires. Even though the ball diameter of Au wire (39 μm) was higher than that of Cu wire (37 μm), the volume of the bonded ball was found to be lower in the case of Au. One possible reason is the softness of Au, which makes Au able to be more easily squeezed into a capillary during the plastic

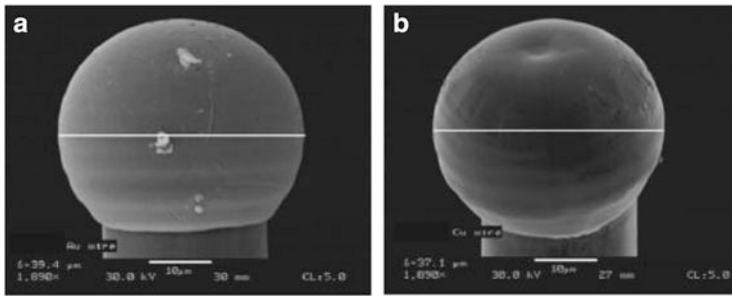


Fig. 2.2 Free air ball (FAB) diameter comparison (a) Au wire: 39 μm , and (b) Cu wire: 37 μm [66]

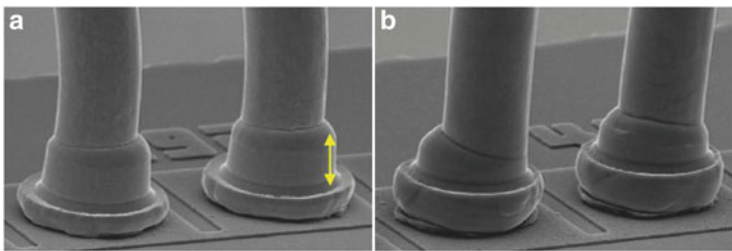


Fig. 2.3 (a) Bonded balls with Au wire, showing a higher height than Cu wire due to a lower bonded ball volume/FAB volume ratio (33 %); (b) bonded balls with Cu wire, showing a lower height compared to Au due to a higher bonded ball volume/FAB volume ratio (64 %) [66]

deformation process compared to the harder Cu. The ratio of bonded ball volume to FAB volume was found to be 33 % for Au and 64 % for Cu. This difference is significant, indicating that most of the FAB was captured inside the capillary for Au wire, whereas for Cu wire, most of the FAB was outside the capillary as a bonded ball. A lower ratio of bonded ball volume to FAB volume results in a taller ball bond for Au wire compared to Cu. The Cu FAB should be made smaller than Au FABs.

Another damage mechanism related to the bonding process is known as Al splash, which is defined as the amount of material displacement outside the bonded ball contact perimeter. Al splash should be minimized, as it can result in shorts with the neighboring terminals. In the case of bonding with Cu or Au wire, the FAB hardness of Cu is 80 HV and for Au it is 60 HV. The bonded ball hardness for Cu is 100–128 HV, whereas for Au it is 70–80 HV. The bond hardness of Cu is higher than the bond hardness of gold due to the strain hardening effect. The hardness of Al is 70–80 HV, which is similar to Au and much lower than Cu, explaining why more splashes were observed while bonding with Cu wire (Fig. 2.3a, b) [66].

The outside edge of the FAB has been found to be harder than the inside of the FAB, since it experiences higher stress and strain during the bonding process [66]. Solutions to minimize the stress on the pad include decreasing the normal force, decreasing the sliding distance, and increasing the hardness of the pad. One way to

increase the hardness of the pad is to use alternative pad metallurgies, including NiPdAu or NiAu. Qin et al. [66] showed the excellent robustness and reliability performance of the Al pad surface in bonding with Cu wire and eliminating Al splash.

2.4 First (Ball) and Second (Wedge) Bond

The formation of a first bond requires deformation of the FAB on the heated substrate by the application of ultrasonic energy and bonding force. The bonding force leads to work hardening, while the ultrasonic energy softens the wire. On the other hand, the second bond is formed by deformation of the wire by the application of bonding force and ultrasonic energy, where the initial microstructural state of the wire governs the wire deformation during bonding. The formation of second bonds has been a challenge with Cu due to its high stiffness and tendency to work harden. The problem is exacerbated by the presence of an oxidation layer on the bare Cu surface, which reduces the wire bondability. Atomic emission spectroscopy conducted on Cu wires in the initial state prior to bonding has showed the presence of copper oxide (Cu_2O) [50]. The formation of copper oxide must be limited by the use of organic coatings on the wire. Additionally, plasma cleaning, typically argon plasma cleaning, must be performed on all substrates within 8 h of wire bonding [54].

The parameters generally optimized for second bonds are ultrasonic bond power (P), bond force (F), and bond time (T). Fujimoto et al. [67] reported the optimization of bonding force and ultrasonic energy for second bond formation. They controlled the wire deformation by varying the bonding force during the initial touchdown phase (initial deformation), as well as during the ultrasonic deformation. They reported that for a 30 μm , 5 N Cu wire, the optimal force during the initial deformation period was 1.4 N, and during the ultrasonic application was 0.4 N.

Cu wire bonding has low units per hour (UPH) because of the longer bonding time for the formation of first and second bonds, compared to Au wire bonding. Mechanical limitations such as heat profile delays, mechanical motion delays, and bonding delays introduce additional delays in the bonding time. Process and bonding time optimization need to be carried out to improve the UPH. A low mean time between assist (MTBA) is mainly caused by non-sticking and short tail. Appelt et al. [68, 69] reported successful implementation of fine-pitch Cu wire bonding in high-volume manufacturing (HVM), where the quality and yield were equal to those of Au wire bonding. Those Cu wire-bonded parts exceeded the standard JEDEC reliability testing specifications by twice the recommended amount. Also, as discussed in section “Bond Wire,” palladium-coated Cu wires are being adopted to address the problem of second bond formation with Cu wire due to the reduced oxide formation at the wire surface.

The formation of stitch bonds on quad-flat packages (QFPs) is a challenge for Cu wire bonding. Ultrasonic energy cannot be used for the stitch processes on QFP packages due to the resonant condition of the lead beams that causes wire fatigue and breakage. A thermocompression scrub is used instead, with a combination of force and low-frequency X–Y table scrubbing [54]. For Cu wire bonding on

pre-plated lead frames, the low strength of second bonds, which is related to the cold forming (high-speed forging process) of Cu wire, is a challenge. Bing et al. [70] conducted vacuum heat treatment of samples at 200 °C for 10 min, followed by wire pull tests and microstructure observations. Deformed grains in the second bonds went through a recovery process, resulting in the bonding strength of the second bonds exceeding the Cu wire strength.

2.5 Wire Bond Process Parameters

The bonding parameters that affect the quality of the formed FAB and the first and second bonds are discussed in this section.

2.5.1 Ultrasonic Energy

Ultrasonic energy is one of the wire bonding processing parameters that determines the bond strength and reliability [27, 55, 71–74]. During the bonding process, the application of bonding force work hardens the bonding wire. Additionally, the high hardness of Cu introduces the risk of underpad damage due to the requirement of higher bonding force. The use of ultrasonic energy lowers the bonding force in bonding by softening the FAB. The ultrasonic energy increases the dislocation density, lowering the flow stress and increasing the wire softness. Thus, the application of ultrasonic energy lowers the wire deformation required for bonding.

Ultrasonic power is directly proportional to bonding wire softening, which in turn determines the bond quality and appearance. Figure 2.4 shows the different failure modes and their occurrence with increasing ultrasonic power for a constant bonding time and force (30 ms/0.392 N). At a lower ultrasonic power, the failure mode is a break at the bond–pad interface. The failure mode shifts to neck break and bond break as the ultrasonic power increases [75].

The optimum ultrasonic power should be determined to achieve good bond quality [71, 76]. Insufficient power has been shown to cause under-formed bonds and tail lifts; however, excessive power can cause a squashed appearance, cracks, and/or cratering damage to the underlying structure on the semiconductor die, resulting in damaged joints [16]. The bondability of copper wire can be determined by the slip area at the bonding interface. The transfer from the slip area to the entire slip can be controlled by the levels of the ultrasonic power and bonding force used. The initial temperature of the preheated chip can also improve the bonding strength [77]. Huang et al. [71] investigated the effect of ultrasonic energy on FAB deformation. He reported that the required ball height can be obtained by lowering the bonding force and increasing the ultrasonic power. This in turn can reduce the stresses on the underpad structure and reduce the possible pad damage. Huang et al. [71] reported that for a ball height of 45 μm (for 50 μm wire), the bonding force decreases linearly as the ultrasonic power increases.

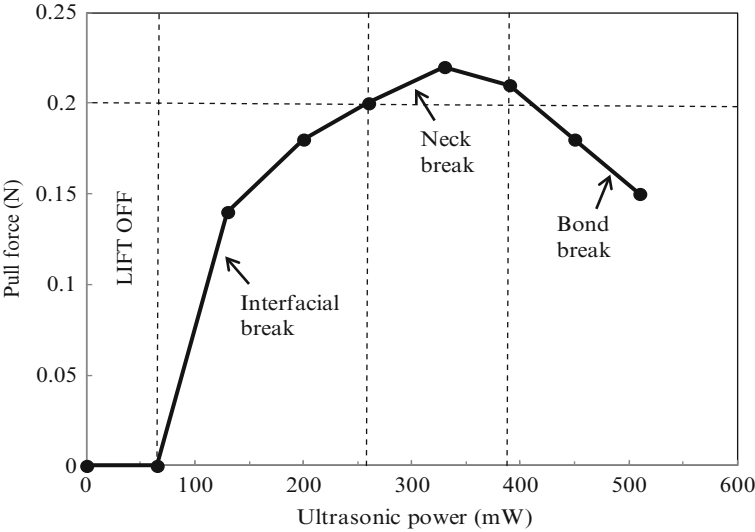


Fig. 2.4 Shift in failure modes as a function of increasing pull force and ultrasonic power (mW) [75]

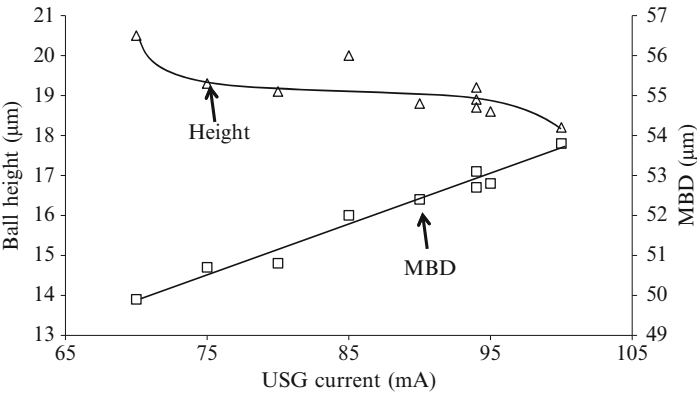


Fig. 2.5 Effects of ultrasonic generator (USG) current on ball geometry [55]

Also, the degree of ultrasonic softening at an ultrasonic power was directly proportional to the ultrasonic amplitude.

The USG current settings must be optimized to achieve good ball bonds. Hong et al. [76] carried out optimization of the bonding ultrasonic power for Cu–Al bonding of Cu wire of 23 μm bonded onto 3 μm thick aluminum–1 % silicon metallization, and reported the optimized ultrasonic energy to be 100 mA. Optimization requires measuring the deformed ball diameter. Zhong et al. [55] reported that, out of all the bond processing parameters, USG current had the most significant impact on ball deformation (mashed ball diameter (MBD)) and reduction in ball height (Fig. 2.5).

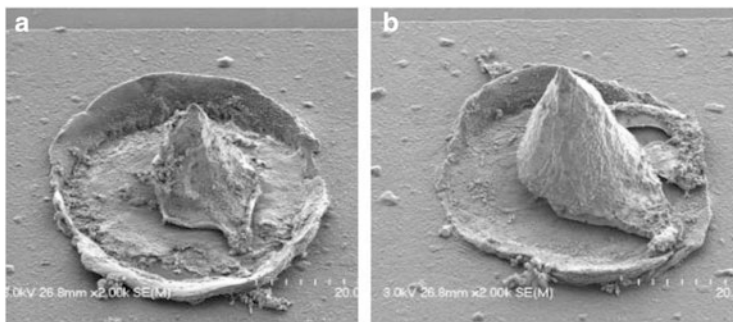


Fig. 2.6 SEM micrographs of Al pads after etching away of the bonded Cu balls: (a) 0 % pre-bleed: more pad splash and pad damage at the edge; (b) 100 % pre-bleed: less pad splash and pad damage [66]

It has been reported that USG current increases bonded ball diameter, ball shear force, and shear force per unit area, and decreases ball height [45, 55]. The shear force per unit area represents how well the micro-weld has been formed between the copper ball and its Al bond pad on an IC chip. When the USG current increases, the shear force per unit area initially increases, saturates over a range, and then increases again. This result suggests that there is an optimum USG current setting in the saturation region of the shear force per unit area. A higher shear force per unit area can be achieved by increasing the USG current (65–105 mA), but this can also cause cratering on the Al bond pad of the IC chip. The optimum USG current should be determined to achieve good copper ball bonds. Clauberg et al. [78] reported the optimization of ultrasonic energy for Cu wire bonding to Al pads based on the Al splash diameter since the Al splash diameter was 4 μm greater than the ball diameter. Additionally, for NiPdAu surface metallization, higher ultrasonic energies could be used at a pitch of 50 μm and upper limit of 40 μm for the ball diameter. Also, ultrasonic energy of up to 115 mA could be used without damaging the underpad structure. In comparison, for bare Al pads, the maximum ultrasonic energy that could be used was 85 mA for 50 μm pitch and 40 μm ball diameter. Ultrasonic energy has been optimized to reduce the underpad stress by reducing the Al splash [27, 71, 73, 74].

Pre-bleed ultrasonic energy is the energy before the impact and is activated when the bonding tool (capillary) achieves the required height. It is applied from the start of contact to the end of impact. If the ultrasonic energy is applied in conjunction with the bonding force during the initial formation and deformation of the FAB, the Cu becomes softer and the ball height becomes less than it would be in the absence of ultrasonic power. Researchers have investigated the use of pre-bleed energy to reduce the underpad stress [71, 74]. Designs of experiment (DOEs) conducted to analyze the effects of pre-bleed have indicated that high pre-bleed settings (>100 mA) decrease Al splash at the edge of the ball [66]. Pre-bleed helps to maintain a flat ball and pad interface, eliminating the concave shape that occurs when pre-bleed is not used (Fig. 2.6). A concave shape is undesirable, since it indicates pad wear near the edge of the bond and poor bonding at the center of the ball. Pre-bleed USG propagates

ultrasonic scrubbing from the ball center to the edge. Other advantages of pre-bleed include elimination of the thinning ring of the Al pad and enabled use of low ultrasonic energy (<90 mA).

2.5.2 Electric Flame-Off Current and Firing Time

EFO current is supplied to form an FAB [79] during the first step in the wire bonding cycle. The heat-affected zone (HAZ) is the wire portion near the ball that undergoes annealing during the firing process. The length of the HAZ depends on the magnitude of the heat-flux during the firing process. Under heat, the grains in the HAZ grow, and as a result, they have different mechanical properties than the rest of the wire. The HAZ affects the wire loop height, wherein a lower HAZ is required to attain a lower loop height. The EFO current and firing time must also be optimized to minimize the HAZ. As the EFO current and firing time decrease, the HAZ length decreases. With the increase in current, the arc duration required to form the FAB decreases. The decrease in arc duration, in turn, results in less available time for the effect of heat to penetrate axially along the wire away from the ball. Since the metal has a finite diffusivity, the length of penetration of the heat effects decreases with higher currents [80]. It has been reported that an increase in the EFO current reduces the HAZ length and increases the deformability of the ball [65, 81, 82]. Zhong et al. [55] reported that a FAB with a higher EFO had a Vickers hardness (HV) that was 9.28 lower than that with a lower EFO (120.82 HV vs. 114.26 HV). Hang et al. [65] reported that up to an 8 % reduction in the underpad stress can be obtained by using high EFO current combined with short firing time. The EFO current combined with superimposed ultrasonics affects the deformation of PdCu wires [83], where higher current leads to more deformable balls and increases the variation in FAB size and shape, and lower EFO current leads to less variation but higher FAB hardness. The use of ultrasonic energy along with the bond force results in a reduction in the force required for FAB deformation.

The micro-hardness of bonded Cu balls is related to the EFO parameters with softer FABs obtained by higher EFO current. This lower hardness is attributed to the higher maximum temperature during FAB melting due to the high EFO current. Because EFO current and EFO firing time are closely related, it is more appropriate to use firing time as a hardness index for FABs. This would make it less dependent on the diameter of the Cu wire. Therefore, for Cu wire bonding, to achieve a soft FAB and minimize the stress induced during ball bond impact, it is recommended to have a shorter firing time during FAB formation, use a lower contact velocity to minimize the impact stress, and use a higher gas flow rate to provide sufficient inert gas coverage to avoid pointed FABs [55].

The EFO parameters, such as EFO current, FAB diameter, EFO gap length, and cover gas flow rate, have to be optimized for Cu wire bonding [20, 55, 61, 84].

FAB requirements include ball size repeatability (the relative standard deviation (standard deviation/average diameter) $< 1\text{--}1.5$ %), ball-to-wire offset for bonded ball concentricity, and no malformed balls (e.g., pointed or oxidized) [54].

The FAB hardness affects the bondability of the FAB: the harder the FAB is, the more difficult it is to form the ball bond. The FAB hardness, in turn, is determined by the cooling rate during solidification of the FAB. During the solidification and cooling of FABs, a large amount of heat is lost by conduction up the wire, and the heat loss is proportional to the cross-sectional area of the wire. An increase in the EFO current coupled with a decrease in EFO time results in a high FAB temperature and thermal gradient across the FAB and unmelted wire. The resulting FAB has a higher residual stress, dislocation density, and, therefore, hardness [85].

The wire diameter variation affects the ball diameter, but it is not controlled in Cu wire bonding. In general, the ratio of FAB diameter to wire diameter should be between 1.6 and 3, depending on the wire diameter, EFO current, and firing time [54]. A higher EFO current leads to better ball size repeatability but a lower number of concentric balls. The optimal settings for the EFO gap depend on the flow head design. A higher gap provides better ball concentricity. The cover gas flow rate also affects the formed ball [61, 86], in that a low rate results in oxidized balls, whereas a high rate results in pointed balls. Based on the wire diameter and type of EFO current, the gas flow rate should be optimized.

For PdCu wires, a larger diameter wire typically has a thicker Pd layer compared to wires with smaller diameters. As the wire diameter gets smaller, the PdCu solid-solution protective layer on the bonded ball becomes thinner. Therefore, there is a higher tendency for smaller wires to have more exposed Cu regions on the bonded balls than larger wires [87]. To ensure protection of first bonds against HAST and PCT, the Pd in PdCu wire has to be distributed over the entire surface of the FABs, forming a protective shield against corrosion attack by halogen ions in molding compounds. Various PdCu wires may have different Pd layer thicknesses over the Cu cores. FABs of different PdCu wires behave differently under the same EFO conditions. Unlike bare Au and bare Cu wires, the FAB formation in PdCu wire has to be optimized individually and is not interchangeable among different PdCu wires. If the EFO parameters are not optimized, dimple FABs and/or inconsistent FABs will be formed [88]. The nonuniform distribution of Pd in the first bonds and the voids associated with Pd-rich phases may contribute to the increase of resistivity and temperature, influencing the formation of intermetallic compounds. Also, the copper ball bond is harder in Pd-rich regions [89].

In Cu wire bonding, the standard FAB diameter is typically 2–2.5 times greater than the wire diameter. More energy is needed to melt the copper tail to form a standard FAB ball, as compared to Au wire bonding. Hang et al. [90] investigated the FABs formed under different EFO conditions (Fig. 2.7). They reported that the FAB formed by Cu wire of 50 μm diameter with an EFO current below 120 mA did not meet the FAB requirement of symmetrical shape and surface. The symmetry of the FABs was defined as the ratio of D_A and D_B as shown in Fig. 2.7.

One of the causes of FAB defects is nonhomogeneous cooling or oxidation. Cu wire requires higher EFO current than Au wire. The resulting higher temperature could cause a sudden expansion of the forming gas around the FAB. During the wire bond cycle, if the forming gas supply is insufficient, the oxygen surges into the glass tube through the hole where the capillary passes, resulting in oxidation of the FAB [91].

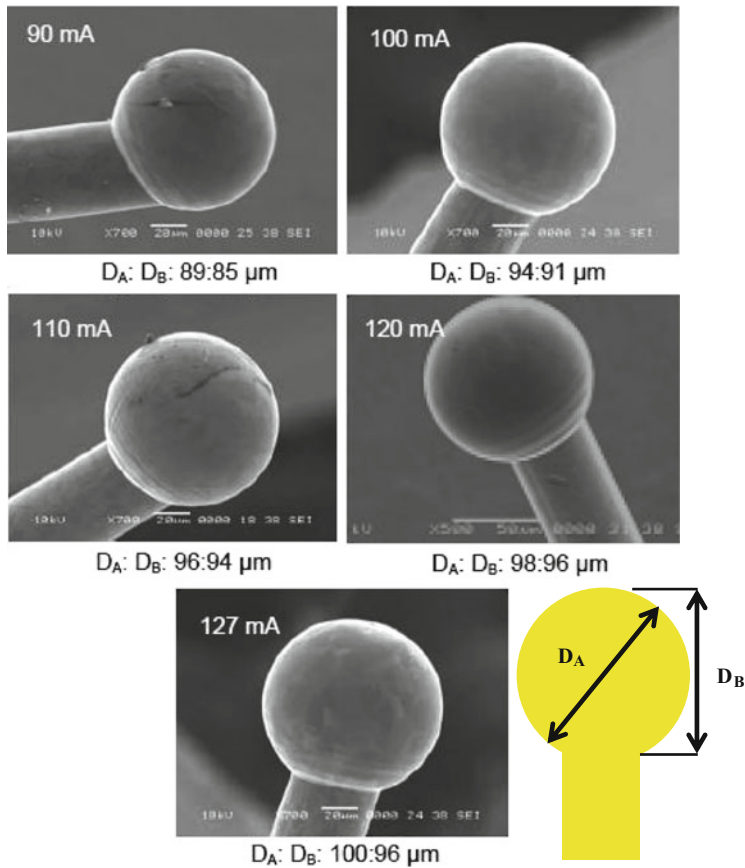


Fig. 2.7 SEM images of Cu FABs formed with different EFO current settings (90–127 mA) [90]

A slow flow rate causes an asymmetric shape of the FAB [85] and thus is unacceptable from a reliability standpoint [90], as shown in Fig. 2.8.

Pequegnat et al. [85] investigated the effect of gas flow rates and reported that the convective cooling effect of the cover gas increased with a flow rate up to 0.65 l/min, and the EFO site showed a 19 °C decrease in temperature. Flow rates higher than 0.71 l/min result in FAB oxidation due to the change in flow from laminar to turbulent. The addition of hydrogen to the cover gas reduces the oxidation of the FAB and provides additional thermal energy during EFO. Jiang et al. [91] carried out an experiment to optimize the forming gas flow rate and EFO settings to target Cu FABs that were 45 μm in diameter. They reported the optimum gas flow rate to be 0.5 l/min. A flow rate lower than the optimum level leads to partially oxidized and distorted FABs. A flow rate higher than the optimum level (0.5 l/min) leads to a strong convection effect, leading to pointed balls. Based on the wire diameter and type, the EFO current and gas flow rate should be optimized.

In a study by Stephan et al. [58], the comparison of bare Cu and PdCu wires showed that at a high EFO current setting (60 mA for FAB diameter of 40 μm and

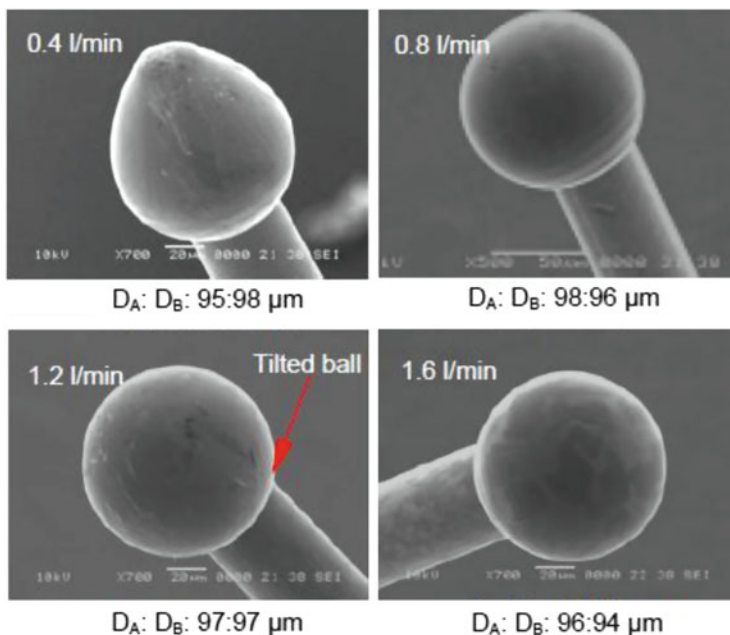


Fig. 2.8 Cu FABs formed at different inert gas flow rates [90]

wire diameter of 20 μm), FABs with bare Cu wire have higher hardness than PdCu wire caused by having smaller grains. For PdCu wire, varying the EFO current (30, 60, and 120 mA) varies the hardness because of the different distributions of the PdCu alloy in the FAB [58]. The dependence of the Pd-distribution on the EFO current suggests that the temperature rise during the EFO current firing is high enough to soften the Pd and cause it to distribute around the FAB, but the temperature is lower than the melting point of Pd (1,554.9 $^{\circ}\text{C}$). To investigate the presence of Pd, analytical methods, such as energy-dispersive X-ray spectroscopy (EDS), can be used. Another way to investigate the presence of Pd is to use a chemical etching solution such as ferric chloride (FeCl_3) to etch away the Cu and leave the Pd. Several reports have been published to investigate the presence of Pd in the FAB and at the bond-pad interface [58, 92], but limited studies have been conducted to investigate the effect of Pd concentration mapping on bonding strength or the effect of EFO on bonding strength.

A comparison of N_2 and forming gas for PdCu wire (15 μm) showed that forming gas is superior to N_2 , since it is not sensitive to changes in EFO (FAB diameter relative standard deviation = 0.94; ball-to-wire offset = 0.53 μm) [54]. When comparing the FAB strength for Cu and PdCu wires bonded in nitrogen or inert gas (forming gas), no significant difference was observed between the two gases for similar EFO currents and energies [93], as shown in Fig. 2.9. It was reported that nitrogen requires 5 % longer than inert gas to achieve the same FAB size. Comparing ball lift, only a minor difference was observed when bonding Cu and PdCu wires in nitrogen or inert gas (Fig. 2.10).

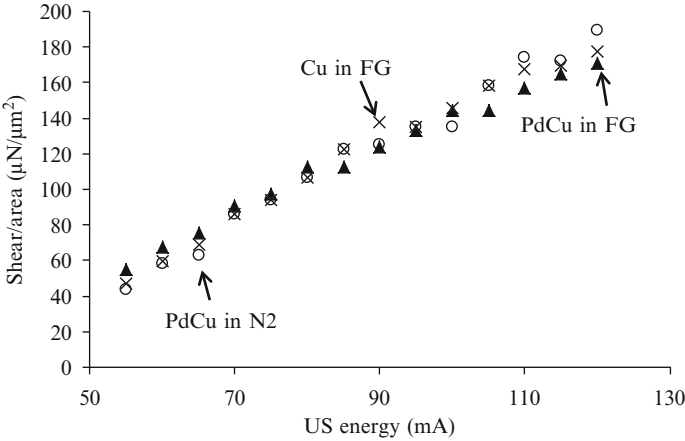


Fig. 2.9 Shear strength for PdCu wire bonded in nitrogen or forming gas [93]

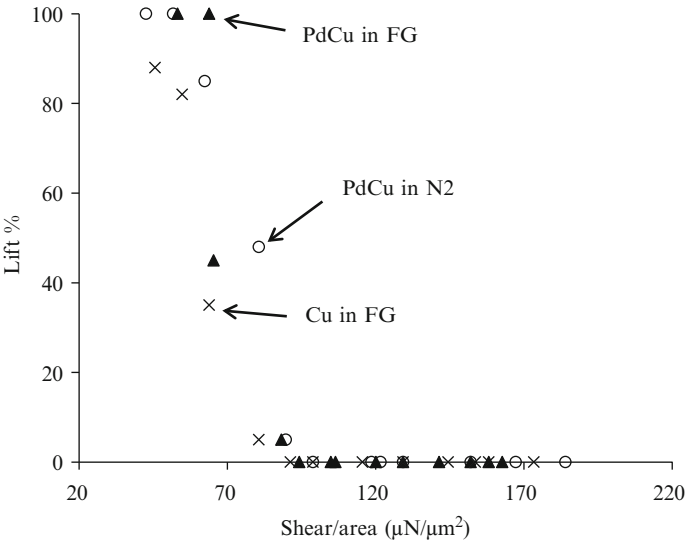


Fig. 2.10 Ball lifts for Cu and PdCu wires bonded in nitrogen or forming gas [93]

2.5.3 Bond Force

The bond force is the downward force exerted by the bonding head during bonding. The bond power is optimized along with the bond force. An increase in bond force and power allows for proper coupling of ultrasonic energy between the bond wire and pad metallization. As mentioned earlier, Cu wire is stiffer than Au wire, which results in higher bonding force requirements compared to Au wire [94, 95].

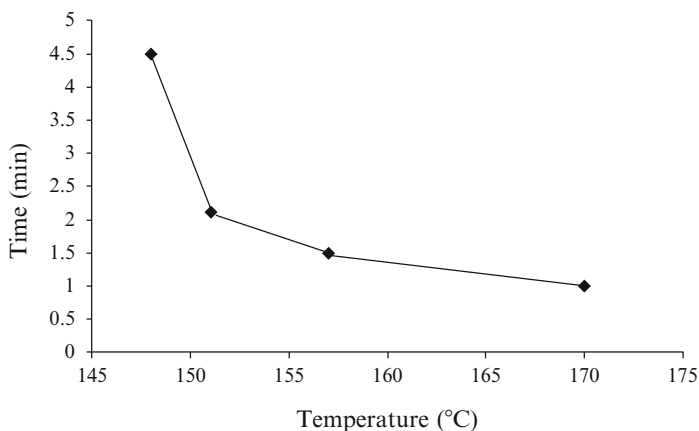


Fig. 2.11 Bonding temperature vs. Cu pad exposure duration [98]

A high bonding force transmits high force onto the bond pads, which is not desirable, since it can damage the pad or cause pad cratering [16]. On the other hand, a low bonding force leads to the nonstick-on-pad (NSOP) condition [96]. Hence, optimization of bonding force needs to be carried out. Hong et al. [76] reported the optimized bond force for shear strength to be 0.589 N for a 23 μm Cu wire with an elongation range of 8–16 % and a break load range of 0.059–0.118 N on a silicon chip $1.06 \times 1.26 \text{ mm}^2$ in size, sputtered with 3 μm thick aluminum containing 1 % silicon.

2.5.4 Bonding Temperature and Time

Bonding temperature contributes to the reliability of the resulting bond. It softens the wire and thus improves the deformability of the wire for bonding. Temperature also affects the deformability of the FAB, which solidifies over a heated substrate. It increases the diffusion at the FAB–bond pad interface. However, high temperatures can result in rigidity loss for board materials, causing bonds to lift due to “ultrasonic cupping.” Ultrasonic cupping occurs when the bonding wire slips out from the contact area between the board plating and the bonding wire during wire bonding. Lee et al. [97] reported a substantial increase in tail bond force and pull force for Cu wire on silver metallization due to a bonding temperature increase from 120 to 240 °C. In another study Hong et al. [76] reported the optimized bonding temperature (for shear strength) to be 220 °C for 23 μm Cu wire with an elongation range of 8–16 % and a break load range of 0.059–0.118 N on a silicon chip with 3 μm thick Al–1 % silicon. The bonding temperature is also known to affect the bondability of the Cu wire [98]. A ball bond was formed on a Cu pad at an interval of 15 s, and the bonding was continued until a no-stick occurred due to the oxidation of Cu pad. At the same time, the bonding stage temperature was varied from 145 to 170 °C (Fig. 2.11). The pad exposure time was an indicator of oxidation time. As seen in

Fig. 2.11, at a bonding temperature of 145 °C, no nonstick was observed even after a pad exposure of 6 min.

Many times, the bond pad temperature is not provided in the literature and the substrate stage or heater plate temperature is specified instead, which is higher than the actual bond pad temperature. For example, Shah et al. [98] measured a bond pad temperature of only 138 °C at a table temperature of 150 °C. As reported by Ramelow [45], comparing bonding temperatures across the literature is difficult because of the difference in the package geometries and thermal conductivities.

Bond time is the duration of the applied ultrasonic energy and bond force. Time has the widest process window; however, excessive bond time can result in slow throughput in manufacturing lines, increased tool maintenance due to contamination buildup and wear, and damaged or burnt appearing wire bonds in areas where the tool contacts the bond.

The optimized parameter values are dependent on various factors, including the wire diameter, pad material, and pad surface cleaning. For a 25 µm Cu wire on Al metallization, the optimized parameters are a bonding force of 0.157 N, a USG current of 90 mA, and a bonding time of 15 ms [22]. Whereas for 23–25 µm Cu wire on an Al pad, the optimized parameters were a bonding force of 0.245–0.451 N, US power of 110–130 mW, and bonding time of 9–10 ms. England et al. [28] reported the bonding parameter-optimized values for a 25 µm Cu wire bonded to Al–0.5 % Cu. The optimized values were a bond force of 0.167–0.334 N, USG power of 90–120 mW, and bonding temperature of 150–175 °C.

2.6 Bonding Process Optimization

The process window for Cu wire bonding is narrower than for Au wire bonding [29]. A good process window for Cu wire bonding can be achieved by designing an experiment that is tailored to the Cu wire bonding process. Bond parameter optimization is aimed at carrying out bonding with no pad cratering or cracking, and 100 % ball bond containment within the pad that is lower than the surrounding metal. Tight capillary control is required to reduce the variation in ball size and facilitate HVM. Another part of process optimization is to obtain adequate IMC coverage [99, 100]. In order to maintain yield, the pad metallization should be cleaned using plasma cleaning to prevent the ingress of foreign particles on the die and substrate prior to bonding.

Process optimization ensures bonding process stability and defines a process parameter window for first and second bond quality [101]. Researchers have adopted several methods for process optimization of Cu wire bonding such as Taguchi methods [102], Six Sigma “define–measure–analyze–improve–control” (DMAIC) methodology [103], orthogonal response surface methodology (RSM) [91, 104, 105], and statistical DOE [105].

Cu wire bond process optimization is essential for bond process stability and the portability of machines and materials. Optimization experiments are conducted to determine the mathematical relationship between the variables and to center the process.

Process centering is also known as finding the process window. The effects of normal process drift can be minimized by centering the process within an acceptable window [106]. Process optimization defines a process parameter window for first and second bond quality.

The common statistical techniques for optimization of the bonding process are DOE, RSM, and contour plots. Wong et al. [105] defined statistical DOE as a way to “encompass methods for the planning, design, data collection, analysis and interpretation of experiments that enables one to effectively and efficiently build the bonding process and use a statistical model between experimental responses and controllable factor inputs.” A DOE helps to determine the most important variable(s) for a process. The center point is a statistical method to determine any possible process drift or instability by providing an estimate of the experimental error. RSM is another technique that is used to determine the optimum empirical relationship between a set of input variables and responses. A combination of DOE and RSM methodologies can optimize the bonding parameters. Contour plots can be used to observe the relation between two input factors and the responses [105].

Researchers have conducted statistical DOE and RSM on common bonding process parameters, such as contact velocity (C/V), bond power, bond force, USG current, and bonding time, to determine the factors affecting the process [91, 105]. Jiang et al. [91] investigated the process window development for Cu wire bonding based on contact velocity, initial force, bond force, USG current, and bonding time. The DOE was carried out based on those input factors, and the response factors were wire pull strength, ball shear strength, and cratering performance on bond pads. The DOE study adopted a half fractional DOE with five input factors to look for factors affecting the model. Based on the results, three factors were chosen for advanced DOE with RSM to obtain the final optimum parameter range.

Wong et al. [105] conducted a DOE to optimize the process parameter window to achieve a ball bond with targeted bonded ball diameter (BBD), bonded ball height (BBH), wire pull, and ball shear strength. The DOE was conducted on bond power, bond force, and bond time to determine the “significant parameters” affecting the process parameter window. The response surface comprised BBD, BBH, wire pull, and ball shear strengths. After the initial screening, full factorial design to determine the interactions between the two significant parameters, bond power and bond force, was conducted. The RSM matrix was used to determine and model the optimum region. Based on the study, bond power was found to be the critical factor in reducing bonded ball diameter.

As an example of bond process optimization (Fig. 2.12), the process window at K&S is determined by the acceptable IMC coverage (generally 80 % or more), Al splash (should not reach the passivation layer), pad crack, and failure site under the pull test (no ball lift or pad peel). It can be seen that Cu wire bonding has a narrow process window due to those considerations.

Su et al. [102] demonstrated the application of Taguchi methods for process optimization and increased the yield from 98.5 to 99.3 %, saving USD \$700,000. Lin et al. [103] used the Six Sigma DMAIC methodology to optimize the material, machine, and bonding parameters, developing a new bonding method of flattening

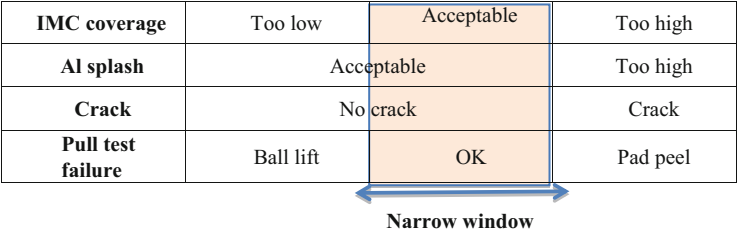


Fig. 2.12 Process window for Cu wire bonding [54]

the bonded ball and applying gentle ultrasonic operation. They also reported that the capillary design and surface roughness improved the wire bond response. Wire coupling with optimum electrical firing parameters and air cushioning can help to achieve robust and oxidation-free FABs.

In addition to bonding parameter optimization, process control for Cu wire bonding manufacturing conditions has to be conducted. Teck et al. [107] conducted a wire floor life control study to determine the usable life of Cu wire after unpacking it from a wire supplier’s seal with inert gas. The capillary touchdown limit for a 47 μm bond pad pitch with a wire size of 20 μm was determined. Capillary degradation started at 200k touchdown, and buildup at the capillary sidewall started at 300k touchdown, causing tail short conditions. Staging on a heater block was also studied to determine the reliability and manufacturability due to substrate outgassing during wire bond heating. The die bonded unit was staged on top of the wire bonder heater block for 0, 15, and 30 min to simulate a scenario where a unit was left on a wire bonder heater until the machine stopped. It was found that substrate outgassing did not affect the manufacturability. The wire pull and ball shear strength showed a reduction after 15 min of staging, but an improvement after 30 min of staging. The improvement was attributed to the interfacial IMC growth due to 30 min of heating at 170 °C. Another way to improve the adhesion of Cu–Al after bonding is to enhance intermetallic growth by heat treatment [108].

Process optimization can improve the bond reliability of specialized die structures such as overhang dies [109, 110]. Kumar et al. [109] demonstrated the process characterizations of different overhang die configurations, where a process was developed for consistent ball shape, remnant Al underneath the bonded ball, and looping across the overhang area. Li et al. [111] developed an approach to reduce the bonding impact on the die by increasing the thickness of the Al pad from 1 to 2.8 μm. The micro-hardness of the bond pad structure decreased by three times, leading to a reduction in the impact and rebound force. The shear strength of Cu wire overhang showed an improvement in the shear strength.

In the process optimization approach followed by K&S, a model-based response-driven approach is adopted, wherein a numerical model is derived from extensive process testing, and bonding parameters are scaled for ball diameter. In order to develop the pitch model for Cu wire bonding, the target ball diameter is set and the bonding accuracy and Al splash are taken into account. After this, the wire

Table 2.3 Optimized capillary, wire and bond dimensions (μm) [54]

Wire Dia	Cap Hole	Cap Chamfer Dia (CD)	Min. Bonded Ball Dia
15	19–20	23–25	27
*20	*24–28	*28–35.5	*36

*most common

size is chosen. Cu is $2.54\ \mu\text{m}$ thinner than Au for the same pitch because of Al splash. Table 2.3 shows an example of the optimized dimensions of a capillary, wire, and bond, as chosen by K&S for Cu wire bonding.

The requirements to achieve quality first and second joints are optimized process parameters, an optimal bonding environment, a contamination-free surface, and proper maintenance of the tool MTBA. The bond pads on an active circuit or a CUP can be damaged if the bonding parameters are not optimized. The main challenges, as mentioned in Chap. 8, are hardness and oxidation. The bonding process needs to be optimized, and parameter adjustments must be made for power, pre-bleed energy, USG current, EFO current, force, and temperature for the Cu wire bonding process. The optimum power should be determined to achieve good bond quality. With increasing ultrasonic power, shear, but not diameter, should increase. The optimum USG current should be established to achieve a uniform ball bond, as the ball deformation and ball shear force increase with an increase in USG current.

2.7 Bonding Equipment

Cu wire bonders require enhanced capability for bonding force and cover gas consumption control. Ramelow et al. [45] reported that bonding companies have developed in-house bonders tailored for Cu wire bonding. For example, ESEC's range of bonders includes the 3100 optima Cu. Similarly, K&S built the Cu wire bonder IConnPSProCu, which contains new, customized hardware with an optimized gas feeding system and high-performance process control. The cover gas feeding system enhances the process window while at the same time reducing the cover gas consumption. Similarly, ASM also provides an automatic wire bonder for Cu wire bonding, Eagle 339Cu, which can bond both fine-pitch and thick wires. The bonder has a special kit to prevent oxidation and has been optimized to minimize the need for forming gas. Cu wire bonding is carried out either with the ball bonder retrofitted with a Cu kit, such as in ESEC (COWI-2), which can perform both Au and Cu wire bonding. The Cu kits contain the system for spooling the wire spools in pure nitrogen and equipment to provide efficient overpressure atmosphere of the forming gas. For example, the ESEC COWI-2 kit is equipped with forming gas flow controls and pressure sensors to keep a check on the gas pressure and flow. Recently, the wire bonder kits include Cu kits such as iConn, the Maxum Ultra, the MaxumPlus, and the 9028 PPS. Other bonders being used are the automatic bonder Eagle 60AP with 138 kHz and the K&S Nu-Tek bonder.

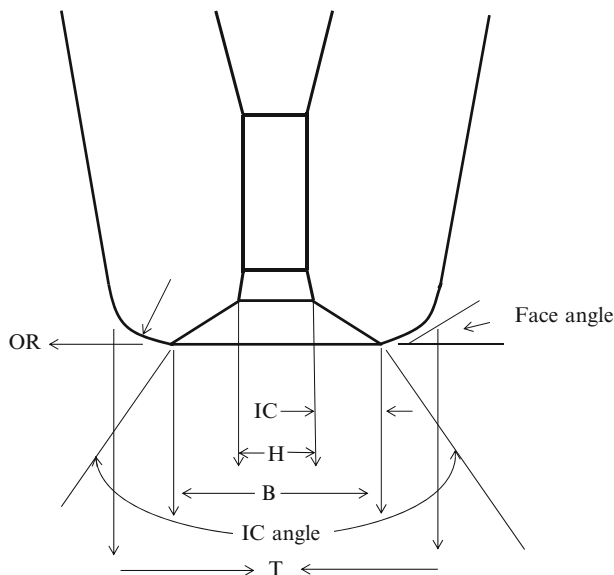


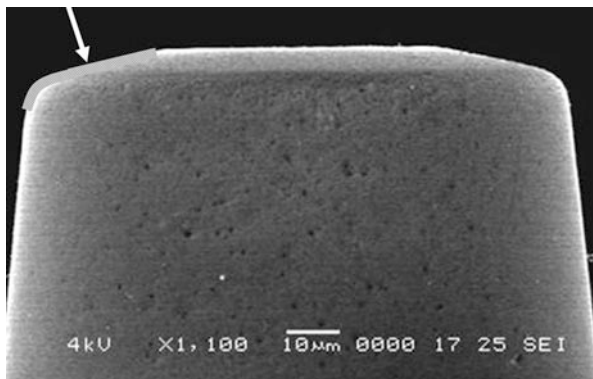
Fig. 2.13 Capillary tip geometry dimensions (tip diameter (T), hole diameter (H), chamfer diameter (B), inside chamfer (IC), inside chamfer angle (IC angle), and outside radius (OR) [112]

In wire bonding, the necessary bonding force and ultrasonic energy are transferred to the wire and the bonding pad/substrate by the capillary to form the bonds. Figure 2.13 shows a schematic of a capillary used in wire bonding. The capillary tip geometry dimensions, including tip diameter, hole diameter, chamfer diameter, inside chamfer, inside chamfer angle, and outside radius, are shown.

The hardness of copper wire is approximately 25 % higher than gold wire, and thus, it is more difficult to bond, especially for lead frame devices. To improve the stitch bondability, higher parameter settings are used for Cu wire than for Au wire, causing heavy cap marks and potential short tails or wire opens. Due to the requirement of higher bonding parameters in Cu wire bonding, the capillaries in Cu wire bonding have short lifetimes: 1000k touchdowns for Au bonding vs. 400k touchdowns for Cu [45]. In addition, Cu–Au stitch bonds are weak. Therefore, copper wire bonding has wire open and short tail defects, low stitch pull readings, and even nonstick on lead.

From the view of capillary design, possible solutions to these problems are optimization of the tip diameter, face angle, and outer radius, and surface finishing of the capillaries. However, the tip diameter is limited by the bond pad pitch of the devices. For example, for a bond pad pitch of 50 μm , the maximum tip diameter allowed is 63 μm . Compared to the standard capillary design, a smaller face angle (8° compared to 11°) improves stitch bondability, but this can also lower stitch pull readings. A smaller outer radius (5 μm compared to 8 μm) also improves stitch bondability, but this can cause heel cracking [113]. The optimization of the capillary design in the chamfer diameter, chamfer angle, and face angle can result

Fig. 2.14 Modified capillary design (the modified portion is shown by the curved line) [113]



in bonding being carried out with lower ultrasonic power and lower bonding force, which results in reduced Al splash and higher shear strength. For improved capillary design, considerations such as surface morphology, physical dimensions, and bonding process window need to be taken into account in engineering evaluations [114]. In order to ensure a long capillary lifetime, the choice of capillary material and its resistance to acoustic impedance are the parameters required to reduce the ultrasonic power requirement [45].

Second bond formation in Cu wire bonding requires the use of granular surface tools to minimize wire slippage during bonding and improve gripping between the wire and the capillary [113, 115, 116]. However, matte or granular finishes have the issue of buildup at the capillary, which reduces the capillary lifetime. The granular capillaries used in Cu wire bonding wear out quickly compared to the polished capillaries used in Au wire bonding. Teck et al. [107] studied the capillary touch-down limit for 47 μm bond pad pitch with 20 μm wire size. It was found that at 200k touchdowns, the capillary started wearing out. At 300k touchdowns, the buildup at the capillary wall resulted in stoppages due to short tail lengths. Therefore, it was recommended that the capillary life of the Cu wire should be controlled at the maximum number of 300k touchdowns to avoid stoppages.

Polished chamfers are used in the second bonds when reduced tip diameters are used and also where the surface bondability is good. Goh et al. [113, 116, 117] developed a capillary design with an enhanced capillary tip surface texture, a larger inner chamfer, a larger chamfer diameter, and a smaller chamfer angle for improved bondability (Fig. 2.14). The modified design led to smaller sized ball bonds, resulting in higher reliability under HTS tests.

Research has shown that the chamfer angle, chamfer diameter, and inside chamfer affect ball deformation [113, 116, 117]. Optimization of these dimensions can improve ball bondability. For example, compared to a standard design, an optimized capillary design has a smaller chamfer angle, a larger inner chamfer, and a larger chamfer diameter, which results in a smaller bonded ball size by limiting the amount of wire material inside the capillary during impact and restricting the softened wire material being squeezed out during wire bonding. About 40 % of the FAB can be contained within the inner chamfer. The new capillary design has been shown to improve ball bondability and small ball size control for ultrafine-pitch

wire bonding [116]. The continuous shrinking of IC chips with closer pad-to-pad pitches has resulted in an increase in demand for special wire bonding capillaries for ultrafine-pitch applications. As capillary tips become smaller, there is a need to redesign the external profiles of capillaries to provide consistent ultrasonic energy transfer during wire bonding [118].

In thermosonic bonding, the capillary vibration amplitude helps determine the reliability of the formed bonds. The maximum ultrasonic vibration should occur at or near the capillary tip for optimal bonding performance. The vibrational behavior of the capillary transmits the ultrasonic energy from the transducer to the interface of the bonding media. Depending on the ball size requirement and the bond power and force settings used, the displacement of the capillary tip during bonding can vary from 0.56 to 3 μm . Higher displacement results in a larger bonded ball size. Depending on the capillary design, the node point can be positioned nearer or farther away from the capillary tip. By moving the node point away from the capillary tip, larger tip displacement can be achieved. Although the vibration amplitude of a capillary depends on the location of the node point, the overall capillary length also affects the vibration behavior. Other factors, such as the internal taper angle, tip diameter, and bottleneck height, also affect the vibration characteristics of a capillary. These dimensions change the displacement amplitude at the capillary tip, which is directly responsible for the bond quality of ball and stitch bonds.

Capillaries with bottlenecks are used for ultrafine-pitch bonding, as their slim profile near the tip can prevent contact with adjacent wires. For wire bonding of low- k ultrafine-pitch devices, relatively low USG power is needed to prevent pad damage. Optimization of the external profile of a capillary can make the capillary transfer ultrasonic vibrations in the preferred direction with low USG power. The ultrasonic vibration displacements of the capillaries were measured by Goh et al. [117] using a laser interferometer. The measurements showed that the ratio of the vibration displacement at the capillary tip to that at the transducer point of a capillary with a small radius transition between the main taper angle and the bottleneck angle was 37 % higher than that of a capillary with a sharp transition, in terms of ball shear (0.102 vs. 0.099 N) and stitch pull strength (0.061 vs. 0.059 N). To solve the ball lift (non-sticking) problem for wire bonding of low- k ultrafine-pitch devices, optimization of the capillary internal profile was attempted [117]. Compared to a standard design, a capillary with a larger inner chamfer, a smaller chamfer angle, and a larger chamfer diameter increased the percentage of the intermetallic compound in the bond interface and improved bondability. Ball lift failure and metal pad peeling were not observed after an aging test. Zhong et al. [118] investigated the effect of ultrasonic vibration on the capillaries with varying zirconia composition and found that the capillaries with the lowest zirconia compositions are most suitable for fine-pitch applications. If the critical capillary dimensions are not optimized, failure can occur. Several failure modes could arise because of incorrect design, selection, and usage of the tool (capillary) or tool wear-out. Table 2.4 provides details about the types of failure modes of wire bonds and their potential root causes.

Table 2.4 Failure mechanisms and potential root causes of wire bond failures

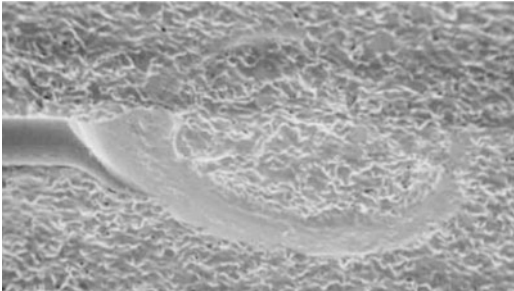
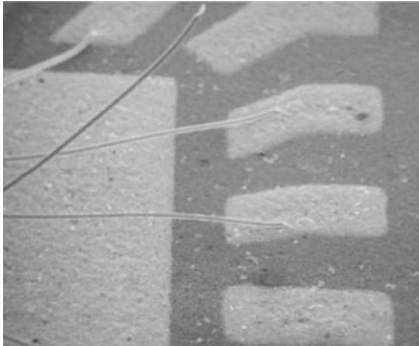
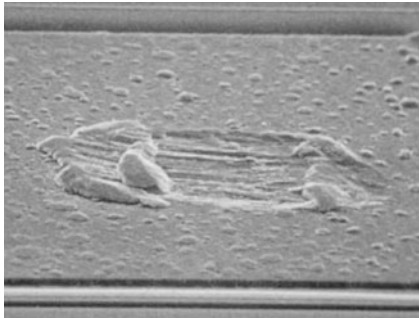
Mechanism	Potential root cause
	Caused by small capillary diameter or worn-out capillary.
	Caused by poor wetting due to poor plating or contamination. Other causes could be improper bonding conditions or capillary dimensions that are too small.
	

Fig. 2.15 Weak, chopped-off, or cut bond [112]

Fig. 2.16 Non-sticking second bonds [112]

Fig. 2.17 Ball bond not sticking to the pad [112]

(continued)

Table 2.4 (continued)

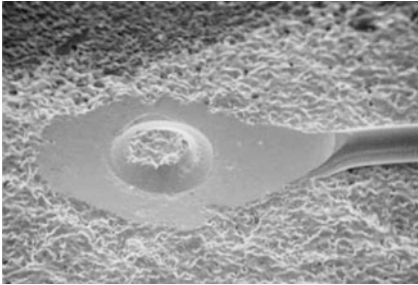
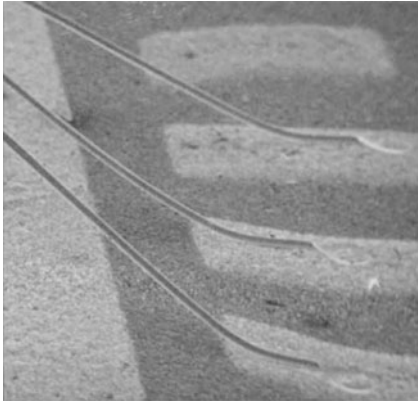
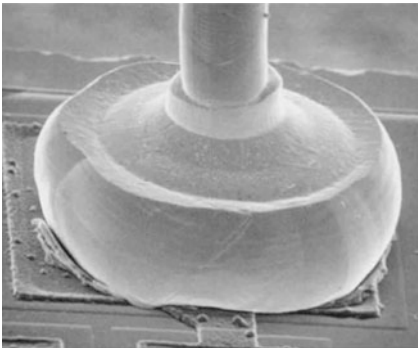
Mechanism	Potential root cause
	Caused by a shallow face angle of the capillary; smaller outside capillary radius compared to wire size, excessive bond force, high-frequency setting, or improper clamping of the substrate.
	Caused by excessive wire length or a wire diameter that is too small for the loop length.
	Caused by a wire or a free air ball size that is too large.

Fig. 2.18 Weak transition from the wedge bond to the wire [112]

Fig. 2.19 Wavy or sagging wire [112]

Fig. 2.20 Larger ball bond than desired [112]

(continued)

Table 2.4 (continued)

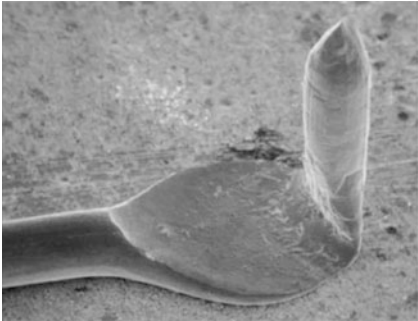
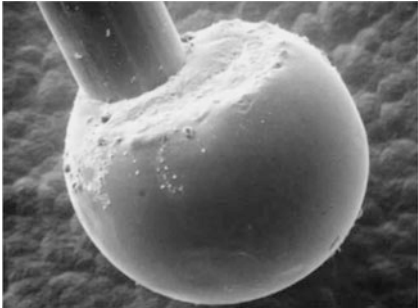
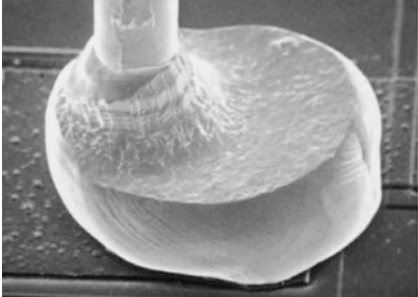
Mechanism	Potential root cause
	Caused by shallow angle causing a strong tail bond and excessive wire length.
	Caused by poor bonding surface, contamination, and excessive wire hardness.
	Caused by poor bonding surface, contamination, and excessive wire hardness.

Fig. 2.23 Golf club bond [112]

(continued)

Table 2.4 (continued)

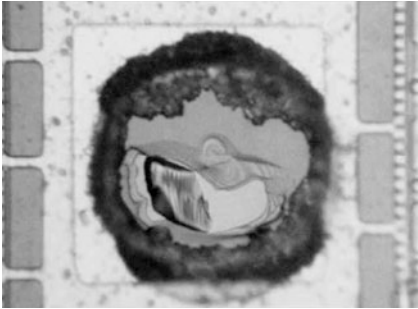
Mechanism	Potential root cause
	Caused by excessive bond energy, poor adhesion of the metal, brittleness of the bond pad, or improper clamping of the substrate.

Fig. 2.24 Pad cratering [112]

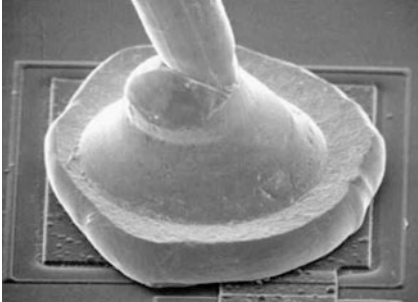
	Caused by insufficient force during bonding, improper bond location, and/or an FAB that is too small.
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Fig. 2.25 Necking above the ball bond [112]

2.8 Summary

In this chapter, the details of the bonding process, including the properties and types of bonding wire, were discussed. During thermosonic bonding, heat softens the bonding wire and the board metallization, and bonding is carried out by adjusting the bonding force and ultrasonic energy. The bonding process must be optimized to minimize defects and form a reliable joint.

The optimum ultrasonic power should be determined to achieve good bond quality. Insufficient power has been shown to result in under-formed bonds and tail lifts. However, excessive power can result in a squashed appearance, cracks, and cratering damage to the underlying structure on the semiconductor die. Ball deformation and ball shear force increase with an increase in USG current. The optimum USG current should be determined to achieve uniform ball bonds.

Other parameters for bonding process optimization include EFO current and firing time, cover gas flow rate, bonding force, and bonding temperature. EFO

current is supplied to form FABs. The micro-hardness of bonded Cu balls is related to the EFO parameters with softer FABs obtained by higher EFO current.

Comparisons of bare Cu and PdCu wires have shown that at a higher EFO current, FABs with bare Cu wire have higher hardness than PdCu wires because they have smaller grains. For PdCu wire, changing the EFO current varies the hardness because of the different distributions of the PdCu alloy in the FAB.

The effect of gas flow rate on FAB formation was also discussed. A slow flow rate causes an asymmetric shape of the FAB, and, thus, is unacceptable from a reliability standpoint. Therefore, based on the wire diameter and type of EFO current, the gas flow rate should be optimized.

The bond force is the downward force exerted by the bonding head during bonding. A high bonding force is not desirable since it can damage the pad or cause pad cratering. On the other hand, a low bonding force is not desirable either, since it leads to the NSOP condition. Bonding temperature softens the wire and thus improves the deformability of the wire and the FAB, and also increases the diffusion at the FAB–bond pad interface. However, high temperatures can result in rigidity loss for board materials, causing bonds to lift.

Bond process optimization is essential for Cu wire bonding, since it has a narrower process window than the Au wire bonding. Researchers have adopted statistical techniques such as Six Sigma DMAIC methodology and statistical DOE for process optimization of Cu wire bonding. Along with the bonding process, the bonding tool could also damage the bond. Several damage mechanisms that can occur due to improper bonding tool usage or dimensions were discussed. To achieve a quality joint, the surface must be contamination free, the tool must be maintained, the process parameters must be optimized, and there must be an optimal bonding environment.

The bonding metallurgy contributes to the overall reliability of the wire bond in that there must be a good metallurgical bond between the wire and the pad/substrate to ensure a robust connection. There are several variations of copper wire and bond-pad combinations used by the industry, resulting in different bond metallurgies. This chapter presents the bond metallurgies associated with copper wire bonding, including bare and palladium-coated copper wire on aluminum pads and on different surface finishes (Au, NiAu, and NiPdAu). These metallurgies are discussed and compared with conventional gold wire on aluminum pads.

3.1 Bare Copper (Cu) and Palladium-Coated Cu Wire

Bare copper wire is used by the industry with different pad finish combinations. However, bare Cu is highly prone to oxidation, causing bondability and reliability concerns. To address this, bonding with bare Cu wires is typically conducted in inert forming gas (95 % N₂, 5 % H₂) to prevent oxidation of the Cu wire. Leong et al. [119] studied the oxidation behavior of Cu wire exposed at 125 °C for 4 h with nitrogen gas, without nitrogen gas, and in a vacuum, and they reported that Cu wire oxidizes under high-temperature storage (HTS) in a nitrogen-free atmosphere.

Oxidation forms an oxide layer on the wire surface. Excessive oxide formation prevents the formation of a round free air ball (FAB), which in turn results in an unreliable joint. An oxidized Cu surface is harder and more difficult to bond with than a non-oxidized surface, which can result in a weak bond-pad interface. Another problem caused by Cu oxidation is the occurrence of corrosion cracks.

One of the ways to address copper oxidation is to carry out the bonding process in an inert atmosphere (as discussed in Chap. 2). This approach, however, requires process optimization, which adds new complexities to the ball bonding process. Another approach is to coat the copper wire with palladium. Pd coating, like any other anti-oxidation coating, must be oxidation free, have good adhesion to the

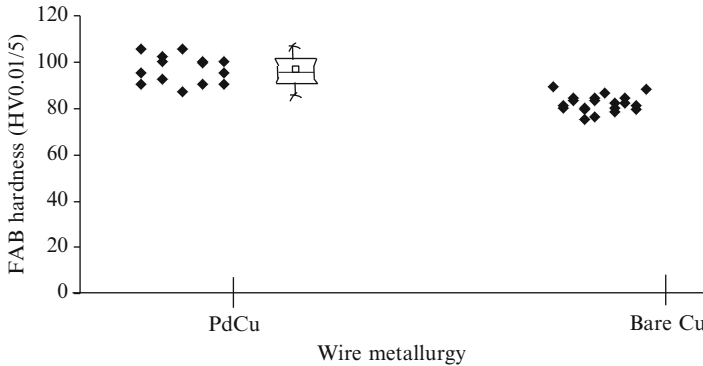


Fig. 3.1 Box plot for FAB hardness of PdCu vs. bare Cu wire (FAB diameter: 40 μm ; wire diameter: 20 μm); electrical flame-off (EFO) current: 60 mA [58]

underlying copper surface, and have good bondability. Cu and Pd are both face-centered cubic and have full miscibility within each other with the formation of ordered phases. Research has found that Pd coating improves bond reliability under humid environments due to the presence of Pd-enriched layers at the bond interface, which limits corrosion [50]. PdCu wires also exhibit better second bond reliability under HTS tests [51]. However, there are other influences on bond reliability due to the Pd coating itself [93, 120]. For example, Fig. 3.1 shows that PdCu wire has higher FAB hardness than bare Cu wire due to the PdCu alloy phase formation in the FAB [58]. The reliability of Pd-coated wires is discussed further in Chaps. 5 and 6.

3.2 Bare Cu Wire on Al Pads

Bare Cu on Al pads is one of the configurations adopted by the wire bonding industry, as of 2013. It has been reported that Cu–Al intermetallic compounds (IMCs) are much thinner (~ 30 nm thick) [121] than Au–Al IMCs (150–300 nm) [122] and have a slower growth rate (10 % that of Au–Al IMCs) during annealing in the temperature range of 150–300 $^{\circ}\text{C}$ [123]. Section “Au–Al and Cu–Al Intermetallics” compares Cu–Al and Au–Al IMCs in detail.

Cu–Al IMCs formed during the as-bonded state are very thin and difficult to resolve under SEM. Xu et al. [121, 124–126] studied the Cu–Al interfacial characteristics by utilizing dual-beam focused ion beam (FIB) and high-resolution transmission electron microscopy (TEM). They experimentally observed a native aluminum oxide layer (~ 5 nm thick) on the aluminum pad (Fig. 3.2), and they reported that the initial formation of IMCs during the bonding process must overcome this relatively inert thin film [121, 122]. The Cu–Al interface in the as-bonded state consists of two distinct regions (Fig. 3.3): a uniform and compact

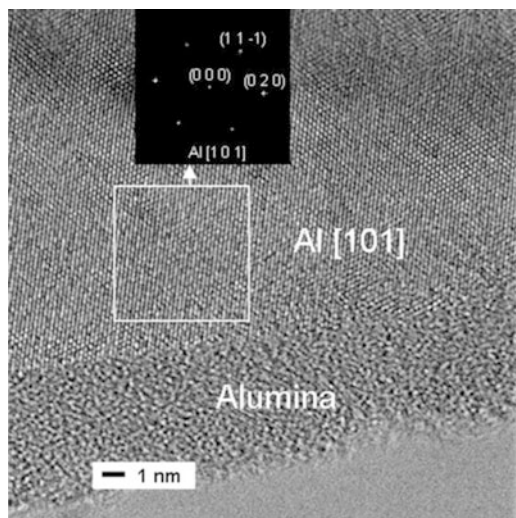


Fig. 3.2 TEM image showing a uniform amorphous native alumina overlayer (~5 nm thick) enveloping an Al pad [122]

alumina layer—a native oxide layer on the Al pad—in direct contact with the Cu, and regions containing IMCs [121, 125]. A uniform layer of aluminum oxide acts as a barrier to the interdiffusion of Cu and Al, so IMCs are unlikely to form in regions with uniform aluminum oxide layers. However, IMCs form in areas where the oxide layer is fragmented during bonding. Those discontinuous Cu–Al IMCs are only ~30 nm thick and have been identified as CuAl_2 by electron diffraction [121, 124–126].

IMC formation is controlled by Cu diffusion and follows a parabolic growth pattern until the Al pad is consumed [124]. The sequence of intermetallic phase transformations during annealing (175–250 °C) was studied and summarized by Xu et al. [126]. In Fig. 3.4, Cu_9Al_4 appears as a second IMC between CuAl_2 (the first IMC that forms during bonding) and the Cu ball. CuAl_2 and Cu_9Al_4 grow simultaneously, where the former is the dominant phase until the consumption of the Al pad (Fig. 3.5). Thereafter, CuAl_2 begins to transform to Cu_9Al_4 due to the dominant supply of Cu and continues to grow by consuming CuAl_2 . Cu_9Al_4 is the terminal IMC. During annealing, the native alumina film (~5 nm thick) of the Al pad migrates towards the Cu ball. A discontinuous aluminum oxide (alumina) overlayer between the CuAl_2 from Cu_9Al_4 remains during annealing. When CuAl_2 has transformed into Cu_9Al_4 upon extended annealing, the remaining alumina is present along the interface between the two Cu_9Al_4 layers [126]. Several researchers have examined the growth kinetics of Cu–Al IMCs [28, 53, 127–129]. The activation energies for the formation of CuAl_2 and Cu_9Al_4 are 60.66 and 75.61 kJ/mol, respectively [126].

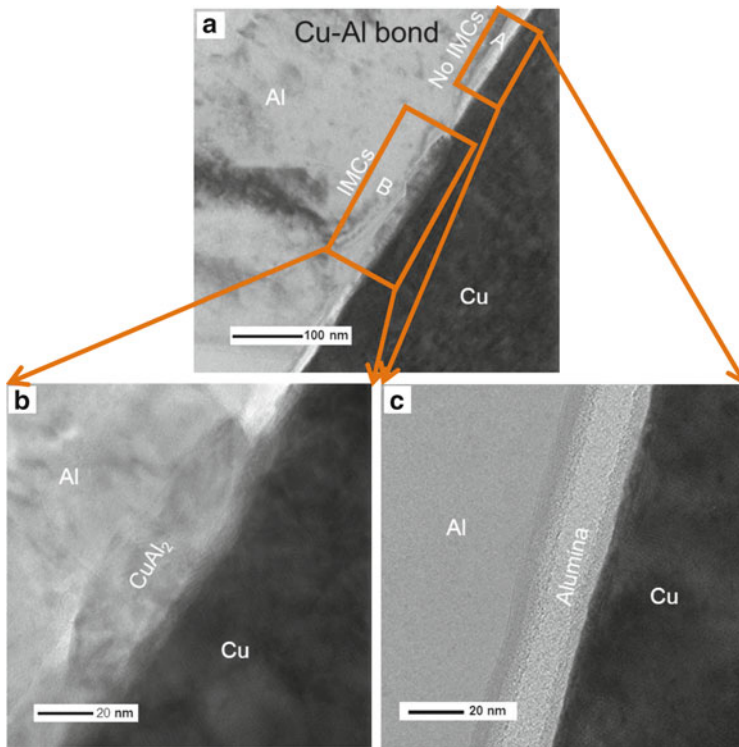


Fig. 3.3 (a) TEM image of the Cu–Al interface in the as-bonded state; (b) details of region B in (a) presenting a CuAl_2 IMC particle; and (c) details of A in (a) showing an aluminum oxide layer between the Cu ball and the Al pad [121]

Cu–Al interfacial metallurgy is influenced by factors such as ultrasonic energy, bonding force, bonding duration, and substrate temperature [125, 130, 131]. The bonding strength depends on the IMC coverage, determined by the extent of fragmentation of a native Al oxide overlayer (5–10 nm thick) on Al pads, which in turn largely depends on the ultrasonic power during bonding. The ultrasonic vibration sweeps away the oxides of Al and Cu, facilitating the formation of a CuAl_2 IMC layer (~20 nm thick) in the areas of direct contact between Cu and Al. Xu et al. [125] reported that ultrasonic vibration causes the local effective temperature at the bond pad to rise to 465 °C, resulting in the accelerated growth of Cu–Al IMCs. In the areas where alumina still remained, the amorphous aluminum oxide layer connected with a crystalline copper oxide.

The bonding duration also influences alumina fragmentation. A long bonding duration breaks the alumina layer throughout the interface. Thus, a continuous IMC layer is formed. Additionally, a high substrate temperature (175 °C) promotes the fracture of alumina and simultaneously increases the interfacial temperature, accelerating the formation of IMCs [131]. Xu et al. [130] examined the effect of pre-ultrasonic energy application on interfacial IMC compound formation,

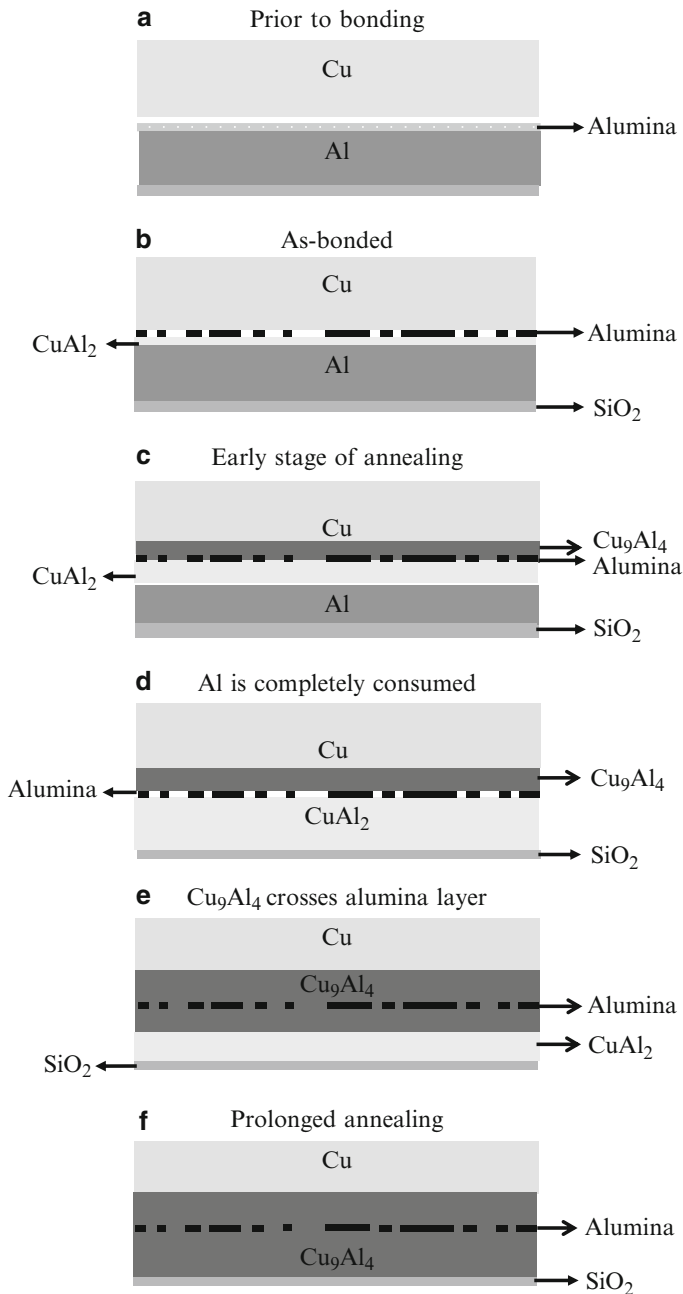
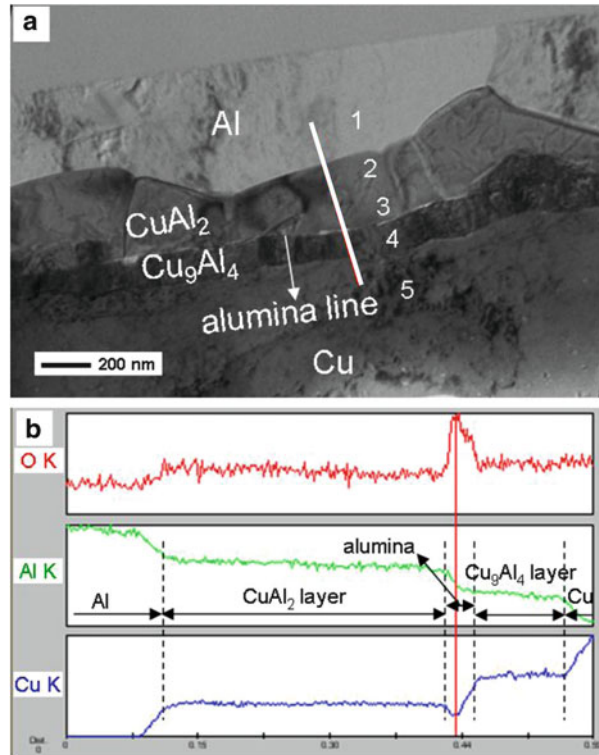


Fig. 3.4 Phase transformation in Cu–Al bonds during thermal annealing: (a) a native aluminum oxide layer on aluminum prior to bonding; (b) CuAl₂ is formed during bonding; (c) Cu₉Al₄ is formed at the early stage of annealing; (d) both CuAl₂ and Cu₉Al₄ simultaneously grow until the Al pad is competed; (e) Cu₉Al₄ keeps growing by consuming CuAl₂; (f) Cu₉Al₄ becomes the only IMC after prolonged annealing [126]

Fig. 3.5 (a) A TEM image of the Cu–Al interface after annealing at 175 °C for 49 h; (b) EDX line scanning results along the line in (a) [126]



reporting that if a pre-ultrasonic energy is applied, IMC formation is initiated in both the peripheral and central areas of the bonds. In the absence of pre-ultrasonic energy, IMCs are only present in the peripheral area.

3.3 Bare Cu Wire on Au- and Ni-Based Die Bond Pads

Cu wire bonding on Au metallization is one combination used in the industry, especially for ultrasonic wedge bonding [132, 133]. As with Al metallization, the higher bonding force in Cu wire bonding causes a reduction of the Au metallization. However, the presence of Cu in the Au metallization due to mechanical mixing during ultrasonic bonding has resulted in good interfacial strength [75].

Bare Cu wire on Ni-based bond pads is another wire–bond pad combination. Compared to conventional Au bonding, Cu wire bonding requires more ultrasonic energy and higher bonding force. Cu wire has the tendency to strain harden when it deforms. Hence, a high amount of stress is transferred to the bond pads and underlying materials during the bonding process. This can result in problems such as damage to the silicon substrate, die cratering, cracking, and peeling of the

bond pads. Ni-based bond pads provide a solution to this problem. Nickel is 1.5 times harder than Cu and four times harder than Al [78]. Thus, it can sustain the high stress resulting from Cu ball bonding and protect the underlying materials against damage.

Devices consisting of low- k active circuitry under the bond pad have exhibited high reliability and no Al splash after employing Ni-based bond pads [23]. Resistance to pad damage is the main advantage of NiPdAu pads: they are resistant to pad splash. Removal of Cu balls using nitric acid has shown that bond pads did not experience pad damage from the bonding process. In addition, no voids were formed at the bond–pad interface, even after 5,000 h at 175 °C. NiPdAu pads outperformed Al pads in all respects: reliability, bond parameter window, bond strength, and lack of pad damage [23]. However, the cost to make NiPdAu pads is much higher than to make Al pads. When Cu wire bonding was conducted on Cu–NiPdAu bond pads with active structures underneath the pads, no damage occurred underneath the bond pads, no obvious degradation of the shear force was found after stress tests, and Kirkendall voiding was not detected after HTS [134].

3.4 Cu–Cu Bond

Cu low- k structures are used in the semiconductor industry because they have lower trace resistance, lower electrical loss, higher electrical current density, and higher speed than the conventional dielectrics in the back-end-of-line (BEOL) interconnects in integrated circuits (ICs) [135]. Cu wire bonding on Cu low- k structures is beneficial both from an economical and an electrical point of view [136].

Bonding on Cu low- k structures is a concern with Au wire bonding due to bonding to a harder metal (Cu) [137, 138] as well as the propensity of Cu to oxidize [139]. Researchers have developed several ways to address these problems, such as argon shielding [140], plasma cleaning to remove the oxide layer [114, 141, 142], optimization of electrical flame-off (EFO) parameters [143, 144], improved capillary design [145], applying metallization such as AuNi or AuPdNi on top of the Cu, applying an organic protection coating such as organic solderability preservative (OSP), and depositing a thin hard brittle inorganic film such as SiN over the Cu surface during wafer fabrication [136].

Cu wire bonding on Cu low- k structures introduces additional stresses on the circuitry under pad (CUP) because of bonding a hard metal on a hard surface. The reliability of assembled packages has been established under common reliability tests, including a temperature cycling test of –55 to 125 °C for 1,000 cycles, HTS at 150 °C for 1,000 h, and a pressure cooker test (PCT) at 131 °C/2 atm for 196 h [146]. Techniques such as finite element analysis (FEA) have been used to assess the stress in the underlying structures [147–151].

3.5 Bond–Pad Interfacial Metallurgies

The reliability of wire bonds in a microelectronics package depends on the morphology and thickness of the IMCs at the bond ball–bond pad interface. IMCs are desirable for forming a good metallurgical bond between a ball bond and the underlying pad. However, increased IMC thickness poses a reliability concern because IMCs have a brittle nature and a tendency to void. Brittle intermetallics and/or the occurrence of Kirkendall voiding due to differences in the diffusion coefficients of atoms can decrease the bond strength and, hence, the bond reliability. Therefore, copper wire can be bonded with several surface finishes. For instance, there could be a Cu–Al interface or Cu–Au interface, depending on the surface finish. This section discusses the intermetallics formed by these surface finishes.

3.5.1 Au–Al and Cu–Al Intermetallics

The solubility of Au or Cu in Al affects the formation of IMCs. Though the crystal structures are the same for these three elements, their atomic sizes are different (Table 3.1), leading to atomic misfit.

The atomic misfit of the Au, Cu, and Al matrix is calculated from the differences in their radii. The atomic misfit for an aluminum atom and a gold atom is -0.7% , while for aluminum and copper it is 10.5% . Hence, movement of an Al atom will be easier in a gold matrix than in a copper matrix. Another factor in IMC formation is electronegativity, which defines the chemical affinity of atoms for solubility. Cu and Al have a lower electronegativity than Au (Table 3.1). Therefore, Al has a higher chemical potential to dissolve in Au than in Cu.

Cu–Al IMCs have lower electrical resistivity and lower heat generation than Au–Al IMCs [17]. The larger size difference between Al and Cu and their lower electronegativity will restrict the solubility of Al in Cu, thus forming thin IMCs [152]. The properties of various IMCs formed with Cu–Al bonding are shown in Tables 3.2, 3.3, and 3.4.

Kouters et al. [153] described the thermal, mechanical, and physical properties of Cu–Al intermetallics, as shown in Tables 3.3 and 3.4 (ρ = density; C_p = specific heat density; α = thermal diffusivity; λ = thermal conductivity; and Θ , η , ζ , δ , and γ are intermetallic phases).

In addition to chemical affinity and electronegativity, heat of formation (HOF) is another indicator of the ease of reactions [22]. HOF is defined as the heat evolved or absorbed during the formation of 1 mol of a substance from its component

Table 3.1 Properties of elements [152]

Property	Aluminum	Copper	Gold
Atomic radii (nm)	0.143	0.128	0.144
Electronegativity (Pauling units)	1.5	2.2	3.1

Table 3.2 Properties of CuAl IMCs [22]

Phase	At.% Cu	Crystal structure	Hardness HV	Resistivity ($\mu\Omega$ cm)	CTE (ppm/°C)	Density (g/cm ³)
Al	0–2.84	Cubic	20–50	2.4	2.35	2.7
CuAl ₂	31.9–33	Tetragonal	324	7.0–8.0	1.61	4.36
CuAl	49.8–52.3	Monoclinic	628	11.4	1.19	2.7
Cu ₄ Al ₃	55.2–56.3	Monoclinic	616	12.2	1.61	NA
Cu ₃ Al ₂	59.3–61.9	Trigonal	558	13.4	1.51	NA
Cu ₉ Al ₄	62.5–69	Cubic	549	14.2–17.3	1.76	6.85
Cu	80.3–100	Cubic	60–100	2.0	1.73	8.93

Table 3.3 C_p , α , and thermal conductivity of Cu–Al IMCs at 20 °C and 100 °C [153]

Phase	ρ (Kg/m ³)	C_p (20 °C) (J/Kg ⁻¹ × K ⁻¹)	C_p (100 °C) (J/Kg ⁻¹ × K ⁻¹)	α (20 °C) (m ² /s ⁻¹)	α (100 °C) (m ² /s ⁻¹)	λ (20°C) (W/m ⁻¹ × K ⁻¹)	λ (100 °C) (W/m ⁻¹ × K ⁻¹)
CuAl	5299	537	560	3.0×10^{-5}	2.3×10^{-5}	87	69
Cu ₃ Al ₂	6278	498	516	8.4×10^{-6}	1×10^{-5}	26	33
Cu ₉ Al ₄	6564	474	498	1.6×10^{-5}	1.4×10^{-5}	50	46

elements. Table 3.5 shows the HOFs for Au–Al and Cu–Al systems for various IMCs. It is apparent that Au reacts more easily to Al (more negative HOF) than Cu.

For the same thermal and mechanical energy, an Au–Al system forms more IMCs than a Cu–Al system. Figure 3.6 shows IMC formation as a function of temperature after 5 h of aging. The Au–Al system forms a thicker IMC layer—namely, AuAl₂, AuAl, Au₂Al, Au₈Al₃, and Au₄Al—than the Cu–Al system [22].

The interdiffusion between the Cu wire and Al pad at the bonding interface during bonding at ambient temperature has been found to be negligible compared to the interdiffusion at the Au–Al interface [17, 28, 29, 123, 152, 154, 155]. As a result, Cu–Al IMCs are extremely thin in as-bonded components and cannot be observed clearly under SEM [156]. Studies using field-emission scanning electron microscopy (FESEM), FIBs, X-ray diffraction (XRD), and TEM [157] have shown the presence of Cu–Al IMCs after bonding. The bonding of Cu wire on Al pads results in the formation of only CuAl₂ particles [121] (Fig. 3.3). In comparison, Au wire forms thicker IMCs upon bonding [122], as seen in Fig. 3.7.

Aging studies for Cu–Al systems have been carried out in the temperature range of 150–340 °C [16, 53, 110, 121, 122, 124–126, 130, 131, 153, 158, 159]. Aging at elevated temperatures has shown less IMCs and slower growth in Cu–Al than in Au–Al. Ratchev et al. [154] compared Au and Cu wire bonding metallurgies for different bond pad finishes for as-bonded and HTS tests. The comparison of activation energies of Au–Al and Cu–Al IMC growth is made in Chap. 5. Microstructural analysis revealed the formation of various Au–Al IMCs due to aging at 150 °C. It was found that, with aging, these IMCs transformed to form new IMC phases. For example, aging for 2 days showed the formation of Au₅Al₃, whereas after aging for 60 days, new IMC phases were observed [154]. Xu et al.

Table 3.4 Thermal, mechanical, and physical properties of Cu–Al IMCs [153]

Intermetallic phase:			CuAl ₂	CuAl	Cu ₄ Al ₃	Cu ₃ Al ₂	Cu ₉ Al ₄
		Units	Θ	η	ζ	δ	γ
Load independent hardness	HV ⁰	GPa	3.94	6.18	5.93	6.25	5.20
Indentation Young's modulus	<i>E</i>	GPa	123.5 ± 6.6	180.2 ± 12.5	180.2 ± 12.5	174.4 ± 19.5	186.8 ± 9.0
Indentation fracture toughness	<i>K_{IC}</i>	MPa√m	0.27 ± 0.66	0.20 ± 0.03	0.21 ± 0.05	0.68 ± 0.15	0.67 ± 0.10
Density	<i>d</i>	g/cm ³	4.27	5.31	5.60	6.25	6.65
	<i>V</i>	cm ³ /g	9.05	8.53	8.44	7.91	7.70
Specific heat density	<i>C_p</i> (20 °C)	J/kg ⁻¹ × K ⁻¹		537		498	474
	<i>C_p</i> (100 °C)			560		516	498
Thermal diffusivity	α (20 °C)	m ² /s ⁻¹		3.0×10^{-5}		8.4×10^{-6}	1.6×10^{-5}
	α (100 °C)			2.3×10^{-5}		1.0×10^{-5}	1.4×10^{-5}
Thermal conductivity	λ (20 °C)	W/m ⁻¹ × K ⁻¹		87		26	50
	λ (100 °C)			69		33	46

Table 3.5 Comparison of heats of formation between Cu–Al and Au–Al IMCs [22]

Gold aluminides		Copper aluminides	
Compound	Effective heat of formation (J/g atom)	Compound	Effective heat of formation (J/g atom)
Au ₄ Al	−18.5	Cu ₉ Al ₄	−3.2
Au ₅ Al ₂	−20	Cu ₃ Al ₂	−4.25
Au ₂ Al	−19.8	Cu ₄ Al ₃	−4.77
AuAl	−16.3	CuAl	−5.44
AuAl ₂	−10.2	CuAl ₂	−6.13

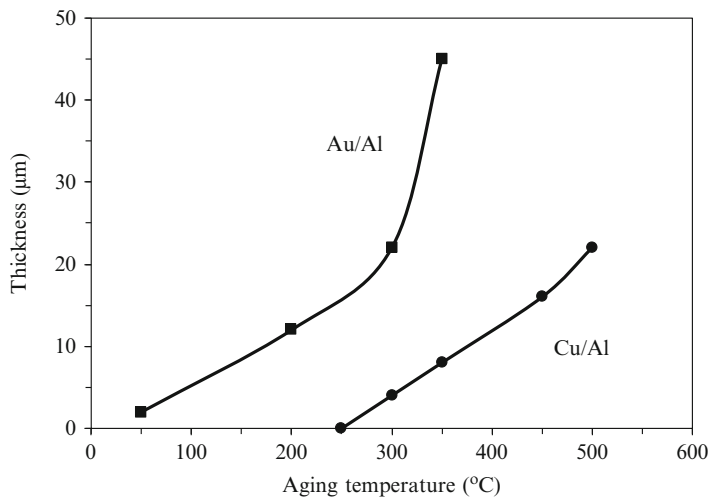


Fig. 3.6 IMC growth with aging temperature ($t = 5$ h) for Cu–Al and Au–Al systems [22]

[122] studied phase transformation at the Au–Al bonds during thermal annealing from 75 to 250 °C using TEM, as shown in Fig. 3.8. Au₄Al and AuAl₂ are the two IMCs formed during bonding. At the early state of annealing, Au₈Al₃ emerges as an IMC between Au₄Al and AuAl₂ and gradually becomes the dominant phase. After the Al pad is consumed, AuAl₂ begins complete conversion to Au₈Al₃. Subsequently, Au₈Al₃ reacts with Au to form Au₄Al. Finally, Au₄Al becomes the sole phase between Au and SiO₂. Au diffuses more rapidly than Al in the IMCs whose growth is dependent on the transport of Au through the course of the annealing process. Additionally, the discontinuous remnant alumina line that exists at the Au₄Al/AuAl₂ interface prior to annealing persists at the Au₈Al₃/Au₄Al interface and migrates towards the Au ball during the growth of Au₈Al₃. After extended annealing, the alumina line continues within Au₄Al.

Kirkendall voiding has been widely observed in Au–Al IMCs [122, 158, 161], but is very sparse in Cu–Al IMCs, as seen in Fig. 3.9 [124, 126]. For Cu–Al bonds,

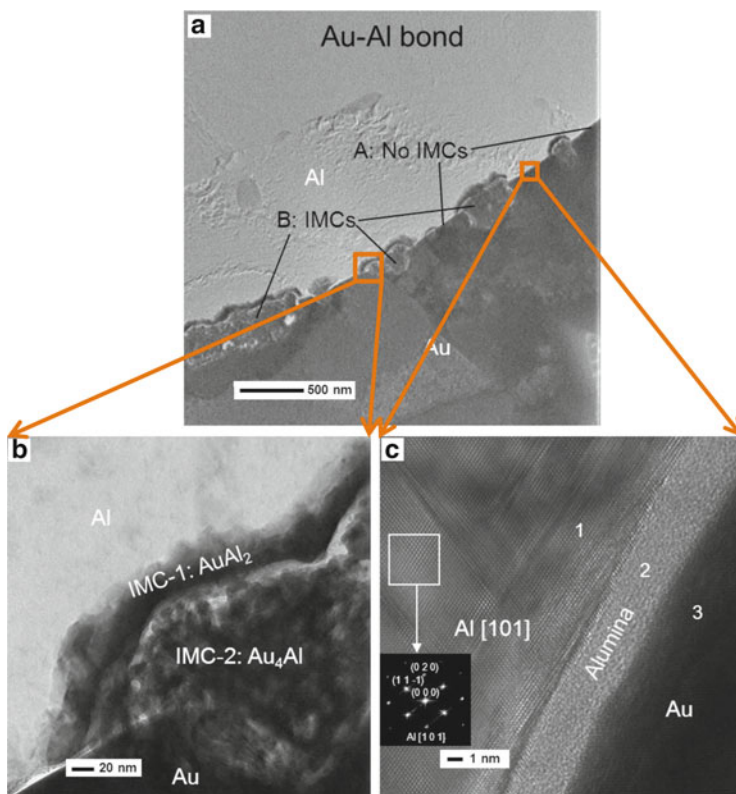
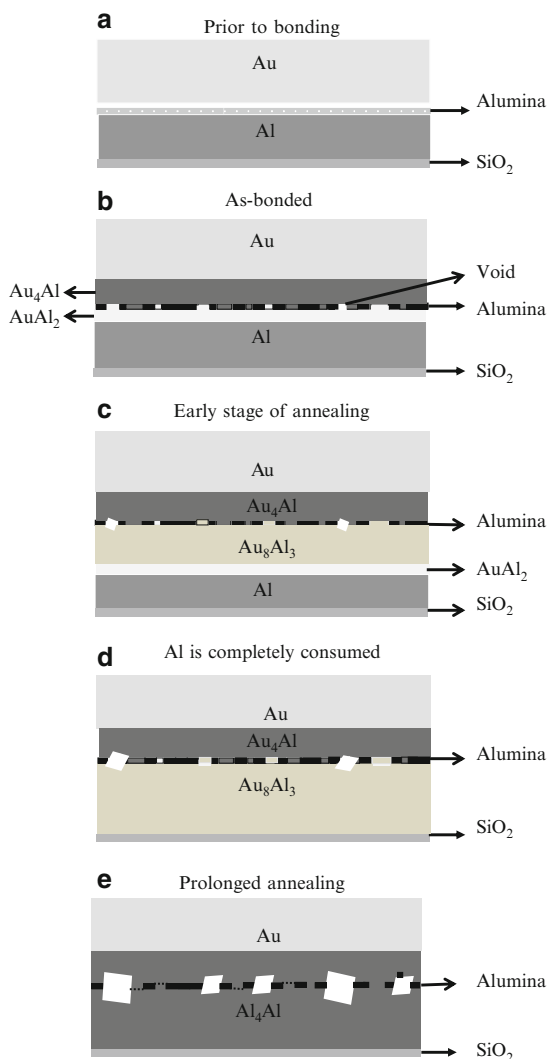


Fig. 3.7 (a) TEM image of Au–Al interface in the as-bonded state; (b) details of region B in (a) presenting Au–Al IMC particles consisting of AuAl_2 and Au_4Al ; (c) details of region A in (a) showing a uniform aluminum oxide layer between the Au ball and the Al pad [122]

only a few voids nucleate and grow adjacent to the alumina after high-temperature annealing, and are usually only tens of nanometers in diameter after annealing at 250 °C for 25 h. There is no voiding after aging up to 200 °C for 2,900 h [155]. In a study by Lee et al. [156], Kirkendall voiding was observed in Au–Al IMCs after 554 h of aging, whereas no voiding was observed in Cu–Al IMCs for the same aging conditions. Based on a TEM observation of void growth during annealing, Xu et al. [158] outlined three mechanisms, volumetric shrinkage, oxidation of IMCs, and Kirkendall voiding, which together account for the coalescence of voids in Au–Al bonds. A volumetric shrinkage of a few percent is associated with intermetallic growth and phase transformations. Intermetallic oxidation occurs at the intermetallics/alumina interface, and the migration of oxygen towards the intermetallics leads to void growth and thickening of the surrounding oxide walls in Au–Al bonds. The formation of large cavities up to 10 μm in diameter in Au–Al bonds after extended annealing at higher temperatures (e.g., 100 h at 250 °C) is attributed to the outward diffusion of Au to react with Al in the area beyond the

Fig. 3.8 Illustration of phase transformation in Au–Al bonds during thermal annealing: (a) a native oxide layer abutting the aluminum pad before bonding; (b) Au_4Al and AuAl_2 are initially formed during bonding; (c) Au_8Al_3 nucleates and becomes the dominant phase at the early stage of annealing; (d) when Al is depleted, AuAl_2 transforms to Au_8Al_3 ; (e) Au_4Al continues to grow by consuming Au_8Al_3 and becomes the end product after prolonged annealing [160]



perimeter of the bonds. This is evidenced by the large amount of IMCs formed outside the bonds [160], as shown in Fig. 3.10. In contrast, the growth of Cu–Al IMCs is much slower than that of Au–Al IMCs, and almost no Cu–Al IMCs form beyond the bond edge (see Fig. 3.10). Therefore, the loss of Cu in Cu–Al bonds is smaller than the Au in Au–Al bonds.

Ratchev et al. [154] reported the presence of Kirkendall voiding at the Au–Al interface after 60 days of aging at 150 °C. As mentioned previously, for Cu wire bonding on Al pads, only ~30-nm-thick IMC particles are present in the as-bonded state. Such metallurgical bonding causes higher initial pull

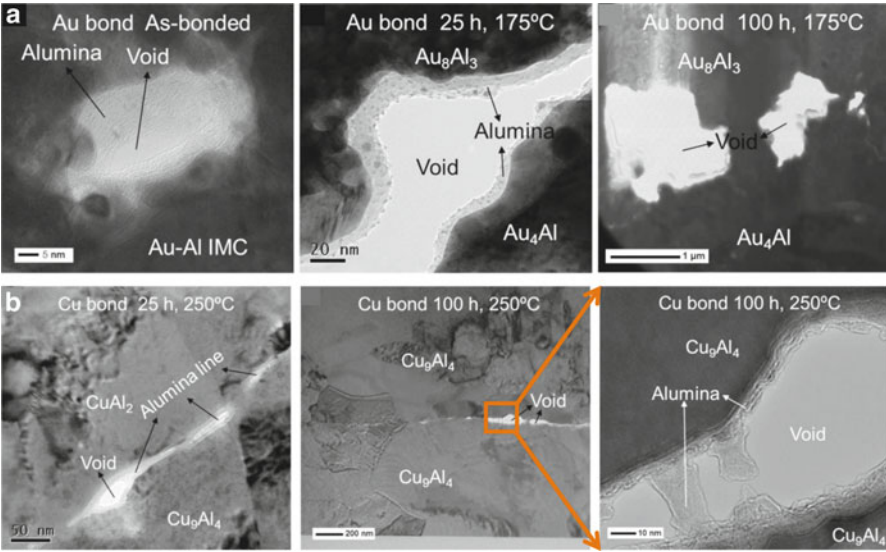


Fig. 3.9 Comparison of voids between (a) Au bonds and (b) Cu bonds [126, 158]

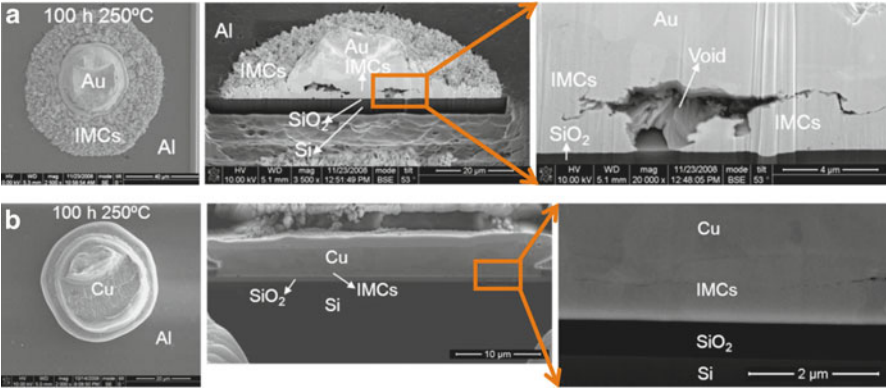


Fig. 3.10 (a) Large voids form at Au–Al bonds after aging at 250 °C for 100 h [160]; (b) minimum voiding observed in Cu–Al bonds for the same aging condition [160]

strength for Cu–Al bonds. Ratchev et al. [154] reported that a thin interfacial layer appeared after aging at 150 °C for 60 days, but it did not occupy the entire contact area. The thickness after 120 days of aging did not change significantly compared to after 60 days of aging. Due to the slow rate of IMC formation at the interface, no voiding was observed. Since the interdiffusion rates of Cu and Al are slow (Fig. 3.11), a higher aging temperature in the

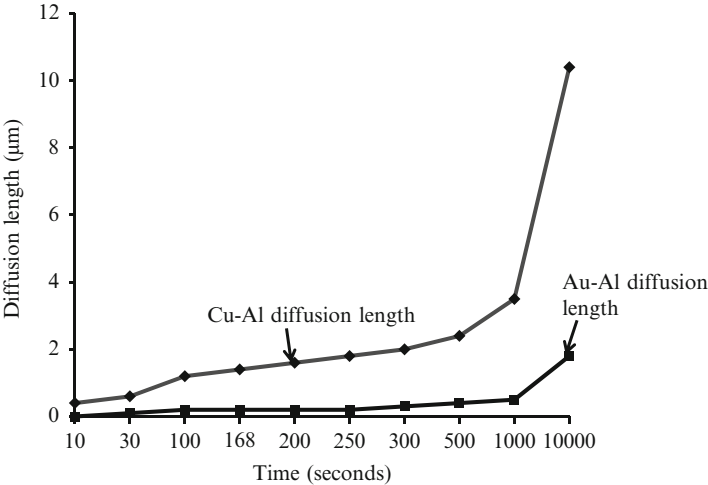


Fig. 3.11 Interdiffusion rate comparison: Au–Al vs. Cu–Al [156]

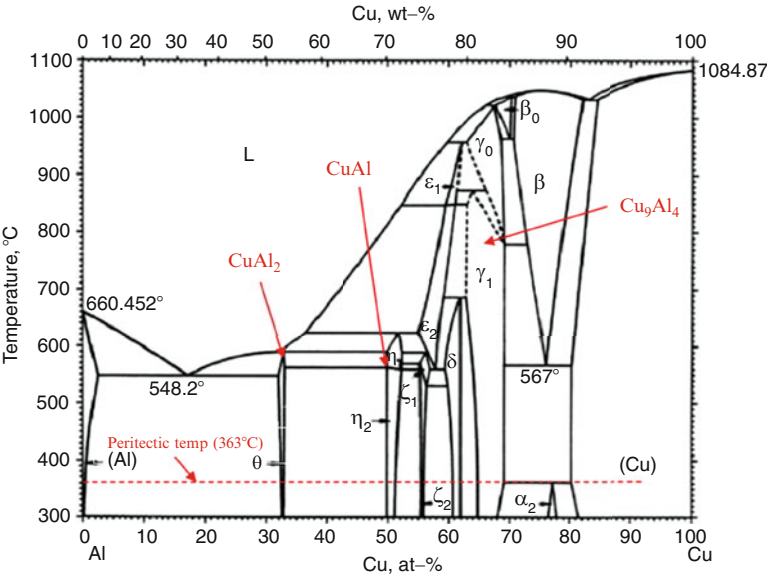


Fig. 3.12 Cu–Al phase diagram [162]

range of 200–350 °C [158] was used to accelerate the growth of IMCs, which resulted in a thin IMC layer after bonding.

Peritectic temperature is defined as the temperature at which the liquid phases in a multiphase system begin to react with the solid phases, resulting in the formation of new compounds. Referring to the phase diagram in Fig. 3.12, the peritectic

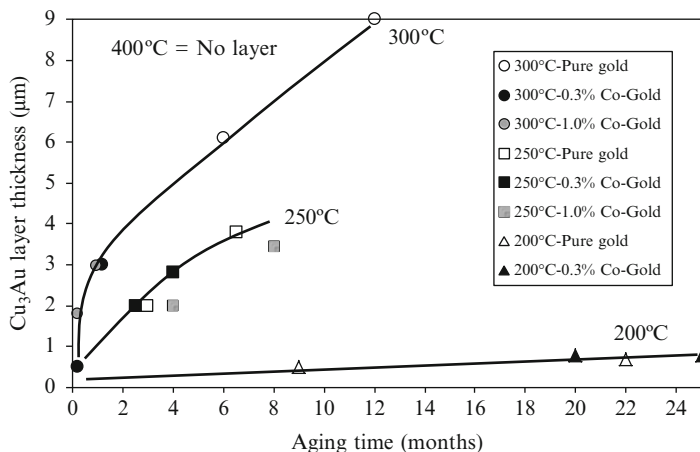


Fig. 3.13 Cu_3Au layer thickness vs. aging time at 200, 250, and 300 °C for Au- and Co-added Cu–Au systems [164]

temperature for a Cu–Al system is 363 °C [123]. Generally, IMCs are stable below this temperature and no longer change with temperature. Therefore, 363 °C is the highest temperature below which Cu–Al IMCs can be accelerated without changing their type. Therefore, HTS tests to accelerate IMC growth (without changing IMC composition) should be limited to below 363 °C.

For a Cu–Al system, rapid growth of IMCs has been reported at 350 °C. At that high aging temperature, CuAl_2 is the first IMC to form in the Cu–Al system, as indicated in the phase diagram in Fig. 3.12. As the copper concentration increases, Cu–Al IMCs begin to appear, followed by Cu_3Al_2 and Cu_9Al_4 . Voiding has also been observed as aging reaches 24 h at 350 °C [123].

3.5.2 Cu–Au and Cu–Al Intermetallics

Cu transport through Au finish occurs via boundary diffusion within 1 h of aging at temperatures of 100–300 °C, with a diffusion coefficient (D) for Cu in Au of $1.64 \times 10^{-20} \text{ cm}^2/\text{s}$ [163]. According to the binary Cu–Au phase diagram, there are three IMC phases— Cu_3Au , CuAu , and CuAu_3 —when the temperature is above 200 °C. Compared to the Cu–Au system, the Cu–Al system involves the formation of multiple IMC phases, namely, CuAl_2 , CuAl , Cu_4Al_3 , Cu_3Al_2 , and Cu_9Al_4 . Kirkendall voiding has also been associated with the Cu–Au system after prolonged aging [164]. For a pure Au system, aging temperatures of 250 and 300 °C caused the formation of a Cu_3Au IMC layer after only 2 months of aging (Fig. 3.13).

3.5.3 Au–AuNi, Au–AuPdNi, Cu–AuNi, and Cu–AlPdNi

Ratchev et al. [154] conducted an interfacial study for Au and Cu wire bonds on Ni-based finishes. It was reported that for Au wire, the Au–AuNi and Au–AuPdNi interfaces did not exhibit IMC formation after HTS tests at 150 °C for up to 120 days. Additionally, no voiding was reported. Cu on AuNi and AuPdNi finishes also did not exhibit IMC formation or voiding upon aging at 150 °C for up to 120 days. Ratchev et al. [154] suggested that the full solubility of the interface combinations of Au, Ni, Pd, and Cu, as indicated by their phase diagrams, is the reason that IMCs did not form. The full solubility of phases in these interfaces can lead to the formation of continuous solid solutions. Also, metal combinations, such as Au–Cu or Au–Pd, form ordered structures that show the same crystallographic structure but have different super lattice unit cells.

3.6 Summary

Bonding metallurgy is one of the factors that determine the overall strength of a wire bond. IMC formation at the wire bond and pad interface is a desirable condition for forming a good metallurgical bond. However, excessive IMC formation can be detrimental to the wire bond strength under high strain rate tests because of the inherent brittleness and propensity to experience voiding.

Due to the propensity of copper to oxidize, oxidation prevention is needed. Bonding with bare copper is conducted in an inert forming gas atmosphere or with Pd-coated copper wires to prevent oxidation. Pd coatings, like any other anti-oxidation coatings, must be oxidation free, have good adhesion to the underlying copper surface, and have good bondability.

In a Cu–Al system, the larger size difference between aluminum and copper than aluminum and gold, in addition to the lower electronegativity of Cu than Au, restricts the solubility of aluminum in copper, thus forming thinner IMCs as compared to an Au–Al system. Additionally, extensive Kirkendall voiding has been observed in Au–Al IMCs, whereas very sparse Kirkendall voiding has been observed in Cu–Al IMCs. Hence, a Cu–Al system has a lower risk of interfacial failures at the ball bond–pad surface interface than an Au–Al system. In order to accelerate the growth of IMCs in a Cu–Al system, 175 °C is used for initial screening.

Cu–Au systems do not have voiding below 200 °C up to 100 h of aging. Additionally, IMC growth below 250 °C is sparse, and reliability risks have not been reported below this temperature.

With the introduction of copper wire bonding, several bond pad finishes have been considered for bonding bare copper and Pd-coated copper wires. For bond finishes such as NiPdAu and NiAu, an interfacial reaction occurs between the copper wire and gold metallization. Studies have reported no IMC formation for Cu on NiAu or NiPdAu wire bond pads. The full solubility type in the interface

combinations of Au, Ni, Pd, and Cu has been suggested as the reason that IMCs do not form for both Au and Cu wire bonds on Ni-based finishes.

The next chapter discusses the evaluation of the copper bonding process, including wire bond quality assurance techniques, failure mechanisms, and material characterization of wire bonds.

In this chapter, tests to evaluate wire bonds and failure modes associated with Cu wire bonding are discussed. Evaluation and inspection techniques for wire bonds depend on the application and the architectural requirements. Bonding inspection is conducted both prior to and after bonding. Evaluation tests can be grouped into subcategories of quality- and reliability-oriented tests. Quality tests include pre-bonding inspection such as visual inspection, machine accuracy checks, and process checks, and post-bonding inspection such as visual inspection and random sampling tests to evaluate bond strength. Bond inspection tests can be nondestructive or destructive, depending on the requirements. Nondestructive tests yield information about the electrical and quality requirements of joints, and destructive tests provide information on the long-term performance and package robustness. The evaluation of wire-bonded devices consists of three steps. The bondability of the die is established first. Then, the bond parameters are optimized and the bond is characterized. The last step is to carry out reliability tests such as the highly accelerated stress test and temperature humidity and thermal cycling tests. Additional evaluations are conducted for special die configurations, such as stacked and overhang die.

4.1 Criteria for Good Bond Formation

“Quality control (QC) is a system of routine technical activities to measure and control the quality of the inventory as it is being developed.”¹ Good bonds can be consistently developed with proper quality control. These controls have to be applied in the process, materials, and design. The following are the process, material, and design controls discussed in MIL-STD-883 [165].

¹ J. Mangino, “QA/QC of inventory systems,” *Good Practice Guidance and Uncertainty Management in National Greenhouse Gas Inventories*, p. 16.

The process controls include making sure that the bond pads are contamination free, that the plating chemistries are optimized to have void-free bonding, that plasma cleaning is implemented to achieve a consistent process, and that the bonding parameters such as bonding force, time, and temperature should be optimized depending on architecture.

Material controls are applied on the bonding wire and wire bond-pad metallurgies. Mechanical properties such as yield strength, ultimate tensile strength, and the endurance limit of the wire should exceed the mechanical thermal cycling stresses. Bonding metallurgies should have good compatibility to form intermetallic bonds and at the same time not form excessively thick IMCs to cause brittle failures.

The wire diameter should not exceed $1/4$ of the pad size for ball bonds and $1/3$ of the pad size for wedge bonds. For ball bonds, in general, the ball size is approximately 2–3 times the wire diameter, whereas for fine pitch and large bond pad applications, it is 1.5 and 3–4 times the wire diameter, respectively. The bond size should be within $3/4$ of the pad size. The loop length and heights should be controlled depending on the process and wire diameter. In the case of wedge bonding, a good bond is achieved when the bond is 2–3 μm wider than the wire diameter. Pads should be designed so that their long axis is aligned along the wire paths.

Bonding inspection is conducted both prior to and after bonding. Sections “Pre-bonding Inspection” and “Post-bonding Inspection” discuss the wire bond inspection practices adopted by the industry.

4.2 Pre-bonding Inspection

Inspection prior to bonding helps achieve a quality bond. Inspection includes examining the bond pads for any damage, such as damage from an electrical probing test, and the bond wire for any defects. An example of pad defects arising from electrical probing is shown in Fig. 4.1. Pads should also be checked for contamination level, oxide formation, and plating chemistry. Inspection of pads can be done visually to detect any scratch marks, abnormal size and alignment of pads, discoloration of pads, and residue from the downstream process. Defects can be located using standard optical techniques. However, it has been reported that some photosensitive residues are not visible in standard light, but can be detected using UV lighting [166].

4.3 Post-bonding Inspection

Several tests have been devised to inspect joints for quality and robustness. These tests include nondestructive and destructive tests. Mechanical tests such as shear and pull tests can be both nondestructive and destructive, and are discussed in Section “Mechanical Tests.”

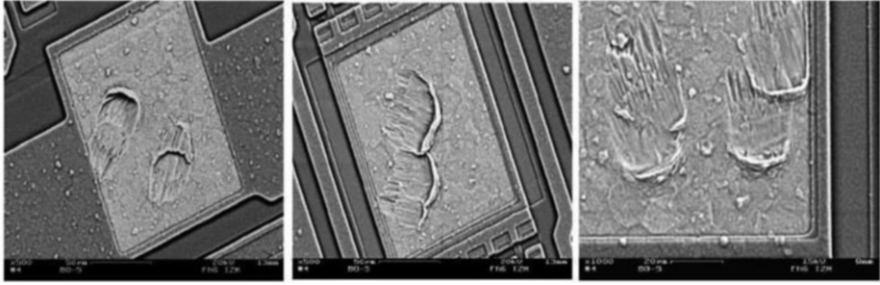


Fig. 4.1 Pad damage (deep or multiple imprints) due to probing [166]

4.3.1 Nondestructive Test

The industry has developed several tests to inspect bonds in a nondestructive manner. Optical inspection has been used to compare bonds with a known standard to detect pad splashing, bond dimensions, and bond deformation. Several techniques, such as scanning electron microscopy (SEM), electron dispersive spectroscopy (EDS), and X-ray imaging, may be used. Due to the decreasing size of bonding wires and high-density wire bonding (e.g., stacked chips), advanced methods such as SEM are popular. Figure 4.2(a, b) shows the use of SEM to inspect wire bonds formed with different powers (higher = 140 bits and lower = 120 bits) and tool force. The bonds formed at higher power are overcompressed [167]. The SEM images of the lower power bonds suggest that this power setting is optimal. An SEM image of a wedge bond with pad splash is shown in Fig. (4.2c). Splash, as explained previously, is caused by excessive bond force and/or power, and is typically greater for softer pads.

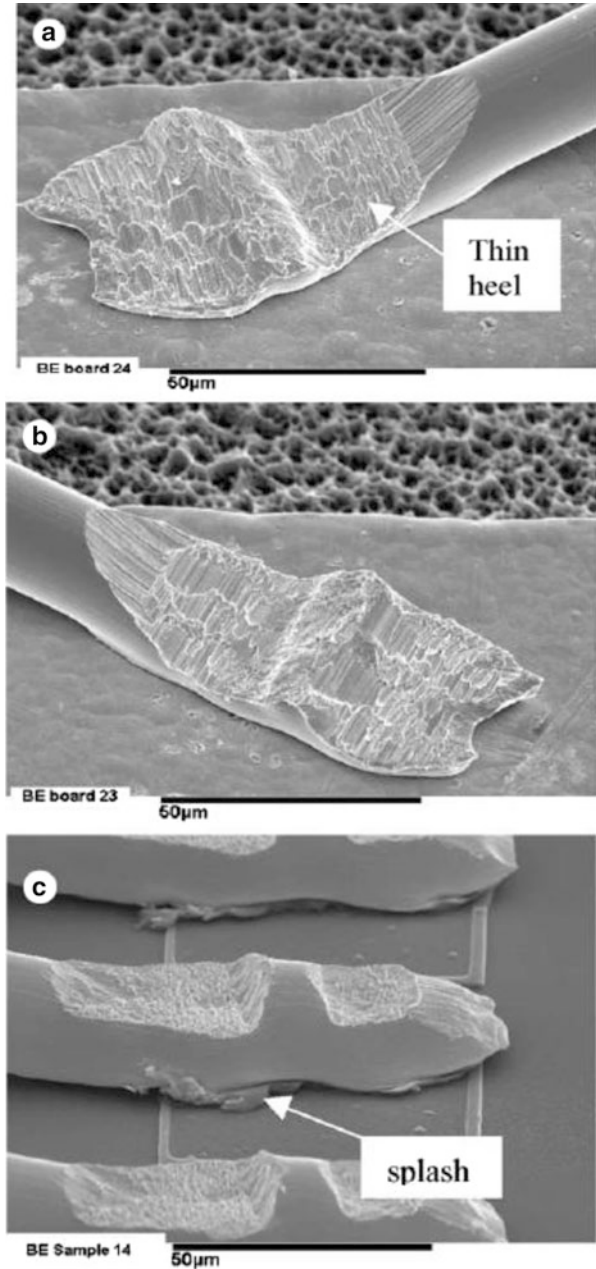
Electrical tests have been developed to check the quality of bonds nondestructively. The aim is to isolate defects and output the electrical parameters to determine the root cause of defects. Defects such as non-sticking pads, discontinuity in wires, open bonds, and shorts between pads due to splash can be determined by electrical tests. Electrical tests such as the four-point resistance measurement method can measure electrical continuity and bond quality. The amount of intermetallics and voiding can also be determined by the electrical test data.

4.3.2 Destructive Tests

Destructive tests investigate bonding quality parameters by carrying out the tests until complete detachment of the bond from the die/substrate/pad. Due to the fabrication cost involved with complex dies, destructive tests can be cost prohibitive. Several parameters need to be measured in destructive tests to detect/evaluate bond defects such as voiding in the bonds, open circuits, cracks, IMC coverage, and type of intermetallic compounds (IMCs). Screening for bonding defects is carried out to eliminate defective joints [168].

Bond etching is a destructive test employed to inspect the layers underneath a bond for damage [32]. Since pad damage is a concern with Cu wire bonding,

Fig. 4.2 A wire on a PCB bonded with (a) high power and high tool force showing high deformation; (b) low power and high tool force showing medium deformation; and (c) die wire bonds showing low deformation [167]



Cu bonds require a different etching procedure than Au wire bonds. Before etching the bond pads, the ball and wire are removed with nitric acid (HNO_3). This prevents the pad from being undercut with HNO_3 , leaving the ball on a thin residual bond pad, which could lead to crack nucleation. The pad is then etched with Aqua Regia (nitric

acid:hydrochloric acid, 1:3) to reveal the dielectric layer. Then, optical inspection is carried out [32]. In bond etching, the ball and pad metallization are removed using chemicals such as potassium hydroxide (KOH) and sodium hydroxide (NaOH).

Pad surfaces can be damaged during the bonding process. Cratering defects are caused by high bonding energy, high bond force, brittle pad materials, hard wire, and/or a non-optimized bonding process. Cratering damage is evaluated by chemically stripping the aluminum metallization to allow for inspection of the underlying oxide layer. Cratering damage is visible in rare instances, but it can be observed indirectly in electrical performance shifts. Cratering damage can act as a path for moisture ingress that can cause mechanical failures.

4.4 Mechanical Tests

Common mechanical tests to evaluate the quality and robustness of joints include shear and pull tests [97, 169]. Shear and pull tests can be conducted for pass/fail qualification by testing the load levels at a predetermined percent of failure load and can be incorporated in production to check for bond consistency.

Evaluation of the bondability and reliability of copper wire bonding involves both the as-bonded reliability and long-term reliability. High-temperature storage is carried out as a preconditioning step before these tests to accelerate interfacial IMC growth at the wire bond–bond pad interface to examine the long-term reliability and then determine the effect of IMC thickness on wire bond strength. In addition, shear and pull tests are also sometimes carried out after subjecting the wire-bonded packages to tests such as mechanical shock and vibration tests, temperature cycling or shock tests, and humidity tests. Table 4.1 shows the typical pull and shear force attributes for different thicknesses of Cu wires. Ball thicknesses as a function of wire thickness are also listed. The following section discusses these tests in detail.

4.4.1 Shear Test

Shear tests can be used to obtain information about the strength of wire bonds. Apart from wire bond strength estimation, the shear test is also used to set up thermosonic ball bonding machines and study the parameters that influence the bondability of devices and package structures [52]. Shear tests are helpful for discovering cratering problems not normally identified by pull testing. The test is performed using a shear tool to push off a ball bond with sufficient shear force.

Table 4.1 Typical Cu wire bond attributes [170]

Specification (μm)	Wire Pull (N)	Ball Shear (N)	Ball Thickness (μm)
18	0.029	0.078	10 ± 3
20	0.039	0.098	11 ± 3
23	0.059	0.118	13 ± 3
25	0.078	0.147	15 ± 3

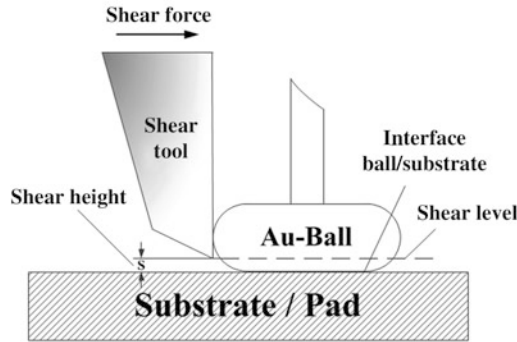


Fig. 4.3 Shear test [166]

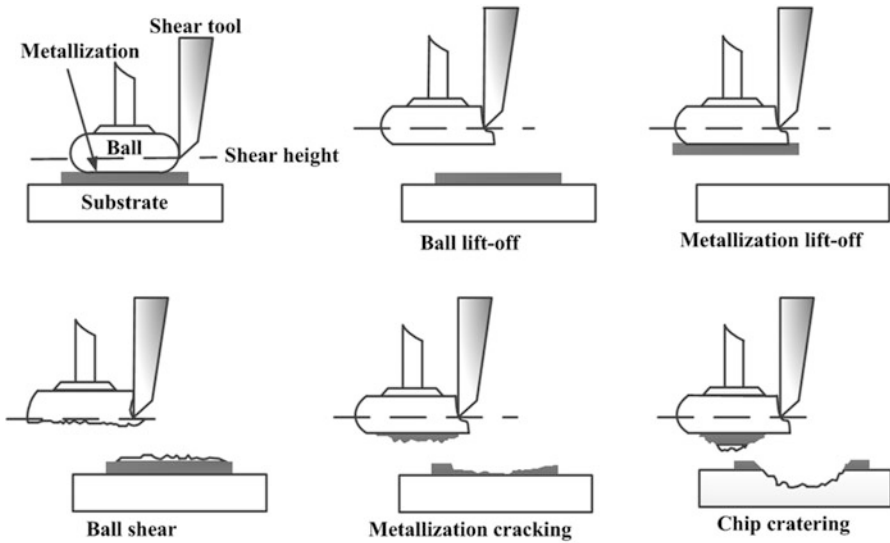


Fig. 4.4 Failure modes in shear test [166]

Figure 4.3 shows a schematic of the shear test conducted on a wire bond. Failure under the shear test can occur by multiple modes such as ball lift-off and pad cratering. Figure 4.4 shows the common failure modes in shear tests. Ball lift-off is defined as a separation at the bonding pad interface with very little or no intermetallic compound present. Ball lift-off can occur where the ball is detached from the pad surface, resulting in failure. Other failure modes include metallization liftoff, ball shear, metallization cracking, and chip cratering. Metallization liftoff is the separation between the bond pad and the underlying substrate. Ball shear failure is when the ram shears the whole ball, leaving the pad metallization or an intermetallic on the bond pad. Cratering is defined as bonding failure as a result of the mechanical damage to the pad or the underlying materials.

Table 4.2 Quality criteria for ball shear testing (thermosonic bonding) [166]

Characteristics	Laboratory	Fabrication
<i>Shear force</i>		
Average value (based on minimum shear force value)	>140 %	>120 %
Standard deviation (based on average value)	<15 %	<20 %
<i>Liftoffs</i>		
Bond liftoff	0 %	0 %
Shear liftoff	0 %	0 %
% Au on pad	>80 % No metallization liftoff, no cratering	>50 %
Minimum shear force (cN)		Ball bond diameter (μm)
15		50
30		75
45		100
75		125

Based on the quality criteria adopted for the shear testing, the tested lots can be rejected or accepted after the shear tests (Table 4.2) for both laboratory and fabrication conditions.

Shear tests should be monitored carefully. For example, the shear speed should be optimized to cause failure at the joint. Shear speeds can change the failure mode, which can lead to misinterpretation of the results. Ideally, if the joints are strong, they should fail in a ductile manner and not through brittle failure. Brittle failure signifies excessive intermetallic formation and a weak interface. Shear tools should be cleaned after every shear to clear away any debris that could affect later shear tests. The height and *x*–*y* position of the shear tool should be adjusted to focus at the center of the bond. If the tool is too high, it can slip, resulting in an incorrect reading. If the tool is too low, the tool could shear the pad instead of the bond, thus producing excessively high shear force values. Statistical methods should be employed to visualize the data and find outliers, which could be test related.

4.4.2 Pull Test

Wire pull is a well-established technique for testing the integrity of wire bond interconnects in microelectronics packages. The procedure for basic wire bond testing is positioning a hook underneath the wire and pulling in the *z*-axis either until the bond breaks (destructive testing) or until a predefined force is reached (nondestructive testing), as shown in Fig. 4.5. Wire bond testing is carried out as per MIL-STD-883 (Method 2011.7 for destructive testing and Method 2023.5 for nondestructive testing).

The locations of common failure modes under the destructive wire pull test are shown in Fig. 4.5 as bond liftoff from pad metallization (No. 1 and No. 5), wire break at bond (heel crack or neck break during ball/wedge bonding, see No. 2 and No. 4), and wire break (No. 3).

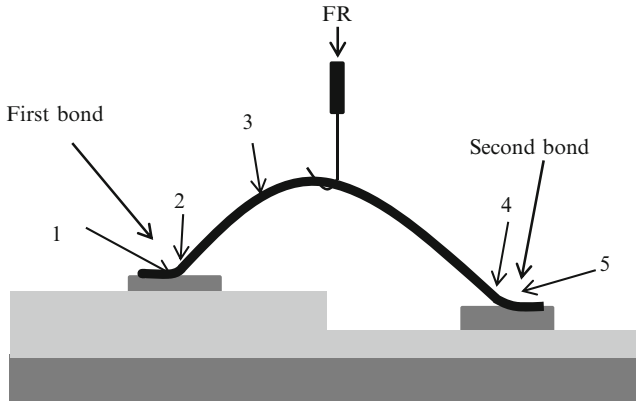


Fig. 4.5 Failure modes in pull test [166]

Ball lift failure is indicative of a weak bond–pad interface, which could either result from a poorly formed bond or a weak bond. Improper wire bonder setup and bond pad surface contamination are the primary causes of ball lifts. Ball neck failure is defined as failure of the wire just above the ball neck and forms the predominant failure mode under pull tests. Ball neck failure is commonly attributed to improper wire bonder setup. Another failure mode in the pull test is wire break at the mid span, which occurs by plastic deformation and ductile fracture. The mid span failure usually gives high pull strength values that are close to the ultimate tensile strength of the wire. Heel break is defined as the severing of the wire from the wedge due to a fracture in the heel. Heel failure occurs due to excessive stresses in the wires that pull the wires away from the bond. It is attributed to improper wire bonder setup. The stresses result in heel cracks, which propagate to fracture. The presence of micro cracks at the heel is one of the major causes of heel fracture, and is attributed to high bonding parameters, and sometimes to damaged capillaries [168]. Weld lift is another failure mode occurring during the pull test, and is defined as detachment of the wedge bond from the bond pad. Weld lift indicates improper bonding process optimization. Weld lift could also be caused by low bond parameters and pad or lead frame contamination.

The nondestructive pull test is a variation of the destructive pull test. In the nondestructive pull test, a fixed minimum pull force is applied based on the required minimum strength. The test is conducted to precipitate failure in the weak bonds while not damaging the strong bonds. The pass/fail criteria can be developed using statistical process capability control. The pull force is usually 10–20 % less than the load to failure. Nondestructive pull test is a good indicator to maintain process control in production with a minimum cost penalty. The load (force, F) distribution on the first and second bonds are equal ($F_1 = F_2$) if $\beta_1 = \beta_2$ (Fig. 4.6).

Various standards contain specifications for acceptance or rejection criteria (see Table 4.3) for laboratory testing and fabrication.

Figure 4.7 shows a plot of pull force vs. bond parameters. It can be seen that it is necessary to optimize the bonding parameters to balance the risk of pull liftoffs and heel cracks.

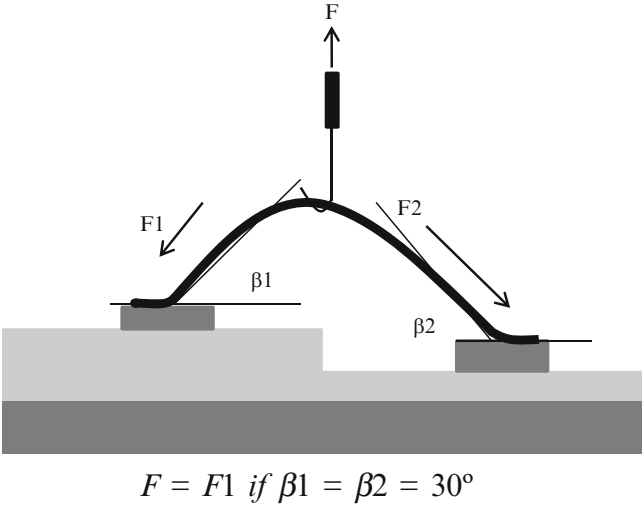


Fig. 4.6 Quality criteria for pull testing [166]

Table 4.3 Quality criteria for pull testing [166]

Characteristics	Laboratory	Fabrication
<i>Pull force</i>		
Average value (based on non-deformed wire)	>50 %	>50 %
Standard deviation (based on average value)	<15 %	<25 %
Proportion of values < (based on standards) cN	0 %	0 %
<i>Liftoffs</i>		
Pull liftoff	0 %	<10 %
Bond liftoff	0 %	0 %

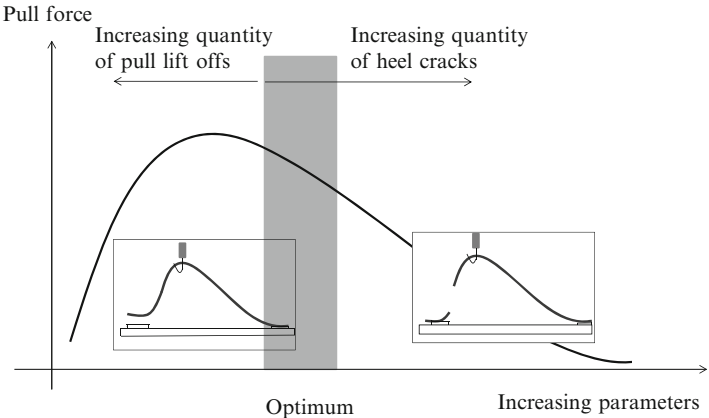


Fig. 4.7 Optimization of pull force parameters [166]

Pull tests are limited because they cannot determine ball strength at the bonded area. Failure under pull testing typically occurs in the ball neck and not at the interface, as the wire diameter is smaller than the ball diameter, and the joint fails at the wire-to-bond connection, which is the weakest interface in the bond.

4.5 Failure Mechanism and Modes

Common failure mechanisms in wire bonding are listed in Table 4.4. The location of the failure indicates the failure mechanism involved with the joint (Fig. 4.8).

Copper oxidizes faster than gold and has a higher modulus than gold; thus, several kinds of damage can be induced on the silicon die during copper wire bonding. The potential failure modes from damage to the silicon die are dielectric cracking, silicon cratering, nonstick to lead frame, weak bonds, and ball nonuniformity. Dielectric cracking and the subsequent leakage failures can be caused by high power and low force, which can damage the underlying oxide in the pad. Silicon cratering is the complete fracture and removal of the pad metallization during bonding. Improper bonding conditions such as high power and low force can cause cratering. Since copper is less malleable than gold, it requires greater force to deform the ball, thus resulting in higher stresses to the metallization. Oxidation leads to poor bond strength and can result in nonstick types of failure, which can lead to ball bond lifting during bonding. Along with high bonding temperatures, low power during bonding can also result in nonstick failures. A weak bond is

Table 4.4 Failure mechanisms of wire bonds [172]

Failure mechanism	Common causes
Break due to bond ball lift: Failure caused at the die–bond interface	Contamination
	Non-optimized parameter settings
	Pad corrosion
	Voiding at pad
	Excessive IMC formation
	Weak metallization
Break at wedge bond: Failure caused at the substrate-to-bond interface	Contamination
	Non-optimized parameter settings
	Oxidized pad
	Damaged pad
Break at bond ball neck: Failure caused around the neck of the ball bond	Non-optimized parameter settings
	Incorrect wire looping
	Die-to-package delamination due to molding
Break at mid-wire	Wire nicks or damage
	Tight wire looping
	Wire sweeping
Shorting (bond to pad and bond to metal)	Non-optimized parameter settings
	Narrow gap between the bond and a metal line on the die

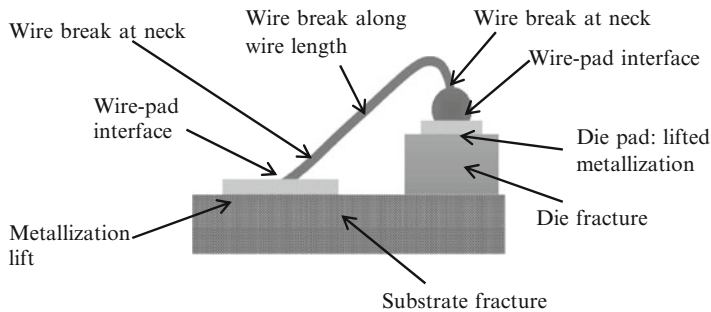


Fig. 4.8 Wire bond failures and locations [171]

characterized by low pull and shear strengths. Probable causes of a weak bond are surface oxidation from high-temperature treatment or poor blanketing of the work area with the inert gas mixture. A ball formed during wire bonding must be spherical in shape so that the bond area can bear the appropriate tensile or shear load. The shape is governed by parameters such as electrical flame-off (EFO), which, if not timed properly, or if not set for the appropriate voltage, current, and polarity, can result in a nonspherical ball.

4.6 Quality Assurance and Testing Methods

Quality assurance ensures a consistent wire bonding process. Typically, defects and failures are caused by an incorrect method (process), material, or machine. Process defects can arise from contaminated pads, defective pads, damaged pads, and non-optimized process parameters such as excessive force, which causes pad damage, pad peeling, and cratering. Material defects can arise from an improper plating chemistry on the pad, resulting in voids in the bond. Voiding in the joint presents reliability concerns. Defects can also arise from an improper machine setup, such as an incorrect tool setup, a non-optimized gas flow rate, and improper bond parameters.

One standard commonly used for evaluating the quality of wire bonding is MIL-STD-883. This standard presents acceptance criteria and bond strength criteria. MIL-STD-883 includes several evaluation methods, such as Method 2011.7 and Method 2023.5, and discusses bond strength. Figure 4.9, which is used in the standard, illustrates bond pull strength as a function of wire diameter.

According to MIL-STD-883, the following defects are not acceptable and are applicable to copper wire bonding [165]:

1. Voids in the bonding pad or fillet area that reduce the metallization path width connecting the bond to the interconnecting metallization to less than 75 % of the narrowest entering metallization stripe width.
2. Intermetallic formation around the periphery of any gold ball bond.

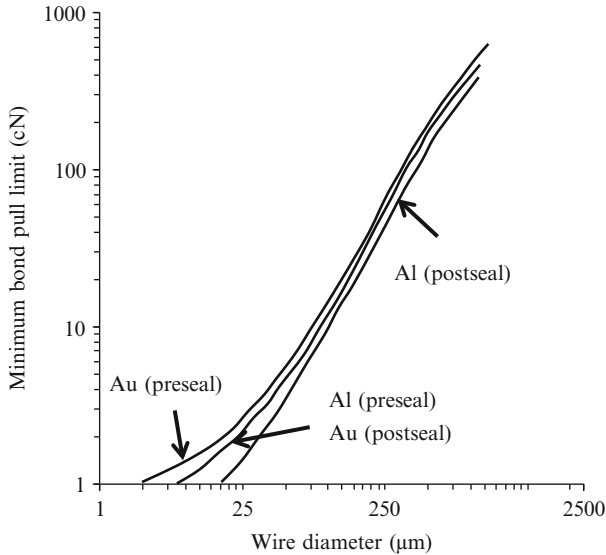


Fig. 4.9 Minimum pull forces for destructive pull test (MIL-STD-883: Method 2011) [165]

3. Ultrasonic wedge bonds on the die or the package post that are less than 1.2 times or more than 3 times the wire diameter in width, or are less than 1.5 times or more than 5 times the wire diameter in length.
4. Thermocompression wedge bonds that are less than 1.5 times or more than 3 times the wire diameter in width, or are less than 1.5 times or are more than 5 times the wire diameter in length.
5. Crescent or stitch bond on the die or the package post that is less than 1.2 times or more than 5 times the wire diameter in width, or less than 0.5 times or more than 3 times the wire diameter in length.
6. Crescent bonds where the bond impression does not cover the entire width of the wire.
7. Bonds where less than 75 % of the bond is within the unglassivated (no passivation layer) bond pad area.
8. Wire bond tails that extend or make contact with any unglassivated metallization.
9. Wire bond tails that extend more than two wire diameters in length.
10. Any wire that comes closer than two wire diameters to the unglassivated die area or the package lid.
11. Nicks, bends, cuts, crimps, scoring, or neck down that reduce the wire diameter by more than 25 %.

Due to the lack of standardized tests and industrial metrologies for Cu wire bonding, companies such as K&S are adopting their own metrologies and target specifications, as listed in Table 4.5. In general, there are lower target specifications for the second bond.

Table 4.5 Target specifications (first bond) [54]

Wire pull	No pad lift, peeling
Shear/area	114.04–144.45 $\mu\text{N}/\mu\text{m}^2$
Cross section	Uniform thickness of Al: Nonuniform thickness correlates to peels in the bake test
IMC coverage	80 % or more
Height/diameter ratio	Below 20 %
Al splash	Al splash should not overlap the passivation layer
Dielectric cracking	No cracking

The propensity to oxidation, high hardness, and strain hardening are concerns for the quality and robustness of first, second, and tail bonds in Cu wire bonding [97]. Hence, bonding process optimization has to be conducted in order to meet the process capability index (C_{pk}) requirement and achieve a wide process window. The lower and upper ends of the process window are defined by the occurrence of ball lift and pad peeling/metal lift, respectively. Variations in wire diameter should be examined, since the break load is proportional to a cross-sectional area of wire. A greater break load causes more peels and lifts. The most common tests to establish the strength of first and second bonds, as well as tail bonds, are the shear and pull tests. Shear and pull tests are performed at time zero and on aged specimens (e.g., aged at 175 °C for 168 h). Usually, the failure data for the shear tests directed parallel and perpendicular to the ultrasonic generator (USG) direction follow a bimodal distribution. A needle pull test (“tweezer test”) is carried out on the wedge side of a wire using tweezers after the ball bond is sheared to determine the strength of the wedge bond.

To assess Al splash, the amount of pad material displaced and ball placement accuracy are measured by visual inspection. In order to pass reliability tests, a sufficient level of remnant Al is required; the preferable thickness is almost half or more than half of the Al pad thickness [127]. Appelt et al. [29] reported the required remnant Al thickness to be a minimum of 100 nm.

Bond etching is carried out to remove the ball and inspect for pad damage. The thickness of the remnant Al and IMC coverage is then measured [59]. The chemicals used for etching are NaOH and KOH. Contrary to the practice for Au wire bonding, where Al is etched to look for IMCs, IMC coverage for Cu is examined by etching the ball away and looking for IMCs on the pad. Typically, high-temperature aging is carried out before ball etching to accelerate IMC growth. After etching, the IMC coverage is examined by conducting IMC measurement. The IMC area divided by the contact area gives the percent of IMC coverage.

Electrical testing is also a measure of the bond quality. Electrical failures in wire bonds are electrical open due to a non-sticking bond, and an electrical short caused by the contact of two adjacent bonds. A four-point probe is one of the techniques to ensure the electrical resistance of the bond–pad interface. Since the interfacial intermetallics formed at the bond–pad interface have higher resistivity than the wire and pad, an

increase in the intermetallic thickness results in an increased resistance. Also, excessive voiding at the interface results in an electrical open. Wire bond quality is also assessed by surface analysis techniques including energy-dispersive X-ray analysis (EDX), wave-length dispersive X-ray analysis (WDX), auger, and SEM.

4.7 Wire Bond Reliability Evaluation

Reliability tests under the actual usage conditions of a product will require long testing times. The testing times can be shortened by accelerating the stress conditions, such as voltage, temperature, and humidity. Additionally, statistical sampling can be conducted to optimize the number of test samples. Acceleration factors are defined by JEDEC [173] as “for a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition.” Reliability tests are conducted under various stress conditions, and an acceleration factor is obtained. The product lifetime under use conditions is then obtained by extrapolating the results to the usage life conditions.

Reliability tests, which will be discussed in detail in Chaps. 5 and 6, evaluate the degradation of bonds over time. Different reliability tests should be performed depending on the application environments [174]. Temperature cycling tests evaluate the long-term electrical performance and thermal fatigue of joints. In this test, samples are exposed to cyclic extreme temperatures to accelerate the failure mechanisms related to mechanical fatigue. Failures include failures of the wire, ball bond, or wedge bond. The root causes of failure can be a weak joint due to insufficient IMCs, contamination on the pads before bonding, and non-optimized bonding conditions. Random vibration and mechanical shock testing is performed to evaluate vibration fatigue-related failure mechanisms in the joint. A frequency sweep determines the natural frequency of the hardware. Vibrations at the natural frequency precipitate weak links in the joint. Thermal cycling and vibration testing can be conducted together to evaluate their cumulative effect under combined loading. Moisture resistance tests are used at the package level with molding compound in the package to detect delamination, which can damage the package under long-term moisture exposure. Electrical overstress tests are conducted to evaluate the current-carrying capacity of the wire after bonding. High current causes current crowding, leading to an electromigration failure mechanism. Bonding metallurgies should be selected to reduce electromigration-induced failures. High-temperature storage tests are conducted to investigate the long-term life of packages exposed to elevated temperatures for a prolonged period of time. Long storage time and high temperatures cause excessive IMC formation, thus degrading the joints. Corrosive environment tests are conducted to evaluate corrosion-related mechanisms, such as those that occur in automotive applications, which are highly corrosive and cause bonds to degrade faster over time.

Molded packages require reliability tests such as temperature cycling (TC), temperature humidity (TH) testing, pressure cooker testing (PCT), and biased

Table 4.6 Molded reliability tests

Tests	JEDEC Conditions	Common Conditions
*HTS	150 °C/1,000 h	
*TC	Cycles –55 to 125 °C: 1,000 cycles	
THB	85 °C/85 % RH/Voltage: 1,000 h	+5V
bHAST	130 °C/85 % RH/Voltage, 3.6 V	Typical +5V, often runs longer, up to 336 h
*uHAST	130 °C/85 % RH: 96 to 100 h	Often runs longer (336 h)
TH	85C/85 % RH: 1,000 h, no voltage	
PCT	121 °C/98 % RH/2 atm for 168 h, no voltage	

*The most common tests conducted by the industry

HAST (bHAST) to assess performance against moisture, electrical parametric shifts, and electromigration. TC evaluates the reliability implications of flexure resulting from differences in the thermal expansion of packaging materials. The failure mechanisms include flexure failure of the wire at the heel, bond pad–substrate shear failure, and wire–substrate shear failure.

For Au, the molded and unmolded reliability are the same because of the non-reactivity of Au with the mold compound. Since Cu is reactive with the mold compound, reliability tests for Cu wire-bonded parts can be divided into molded and unmolded reliability tests. Table 4.6 shows the common reliability tests for molded parts. These tests were originally designed for Au wire-bonded parts and have not yet been qualified for Cu wire-bonded parts. The tests marked with (*) in Table 4.6 are the most common tests conducted by the industry.

4.8 Summary

Evaluation tests and inspection techniques for wire bonds depend on the application and architectural requirements. Good bonds can be developed consistently with proper quality controls in process, materials, and design during production. Bonding inspection should be conducted both prior to bonding and after bonding. Bonding pads can be damaged during an electrical probing test, which damages the pads before bonding and leads to defective bonds. Pads should also be checked for level of contamination, oxide formation, and plating chemistry.

Bond inspection tests are either nondestructive or destructive, depending on the architecture and process requirements. While nondestructive tests yield information about the electrical and quality requirements of joints, destructive tests yield information on long-term performance and package robustness.

Several techniques are presented in MIL-STD-883 to evaluate joints and implement process controls to yield good joint quality. Due to the lack of standardized tests and metrologies for Cu wire bonding, companies such as K&S are adopting their own metrologies and target specifications. Reliability and quality tests identify failure mechanisms, each of which should be documented and prevented to achieve a robust process and package.

Wire bond reliability is evaluated by subjecting bonded parts to temperature cycling or shock, humidity, and electromigration tests. Shear and pull tests conducted after the above tests or high-temperature storage (HTS) tests are also considered reliability tests. In HTS, temperatures range from 150 to 250 °C to accelerate the high-temperature degradation of the wire bonds. High-temperature applications with temperatures above 200 °C require a storage temperature of 250 °C to accelerate IMC growth and interfacial failures, whereas tests for consumer electronics are conducted at temperatures of 150–200 °C.

Reliability tests are followed by inspection tests, such as optical inspection to analyze bond damage, pull strength and shear tests to analyze bond strength, and electrical tests to assess parametric shifts. For PdCu wire, additional failure analysis is conducted to examine Pd distribution in the joint, as the interfacial presence of Pd could cause early failures in reliability testing.

This chapter discusses the high-temperature aging and thermal cycling tests used to evaluate bond reliability. Humidity and electromigration tests are discussed in Chap. 6.

5.1 High-Temperature Storage Tests

A common mechanism of wire bond degradation at high temperatures is the interdiffusion reaction at the bond–pad interface, which results in the growth of intermetallic compound phases. HTS or bake tests are conducted to assess wire bond strength and reliability under high temperature. This section discusses the HTS tests conducted on Cu and PdCu wire bonds and different pad combinations. Comparisons are made with Au wires.

A molded bake test is carried out to assess the HTS life of molded wire-bonded parts.

An unmolded bake test (UBT) is a high-temperature aging test conducted on unmolded Cu wire bonds to accelerate intermetallic growth. The requirement for passing UBT is uniform Al thickness under test. The correlation between the

uniformity of Al thickness and the IMC, shear, or other metrology is also examined. As of 2013, no standards exist for this test, and companies pick the conditions based on their requirements. For example, K&S conducts aging at 175 °C for 192 h in an air or a nitrogen environment. A pull test at the die edge or above the ball is usually conducted for five or ten wires per side of the die, and peels and lifts are counted. The target result is no peels or lifts.

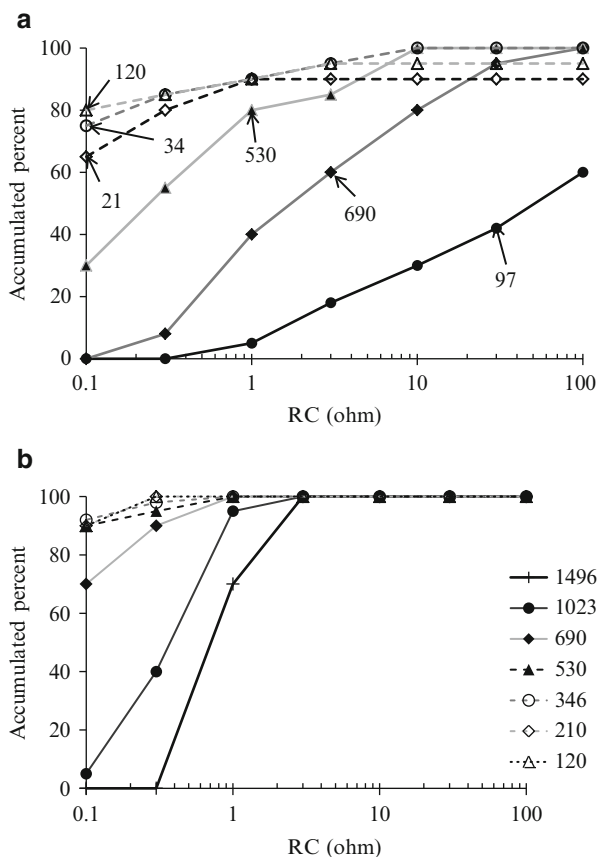
5.1.1 Au Wire on Al Pads

Elevated temperatures lead to enhanced interdiffusion reactions between Au and Al, promoting the transformation of Au–Al phases and the growth of voids. The growth and transformation of IMC phases occur along with the formation of voids inside the bonds at the Au–IMC interface and in Al pads along the periphery of the bonds. The voids are formed as a result of the coalescence of vacancies formed due to the difference between the diffusion rates of Al and Au atoms, known as Kirkendall voiding. The Au–Al intermetallics are more brittle and harder than both Au and Al. During the initial stages of degradation, voiding does not greatly influence the mechanical strength and contact resistance of the bonds. However, after being subjected to high-temperature aging, voiding increases with time and eventually the bond becomes mechanically weak and/or the electrical resistance increases above an acceptable level, thus causing failure of the device [175, 176].

Researchers [175, 176] have studied the effects of high-temperature aging on Au–Al systems. Noolu et al. [175] carried out aging of Au–Al ball bonds at 175 and 250 °C for up to 1,000 h and characterized the Au–Al phase transformations and void growth. Upon exposure to elevated temperature, nucleation, growth, and the transformation of Au–Al phases, the growth of voids was reported. Upon aging at 175 °C for 2 h, two IMC phases, Au_8Al_3 and Au_2Al , were formed. As the aging duration increased to 10 h, phase transformations occurred, resulting in the formation of a new IMC phase, Au_4Al , at the Au–Al interface. Similar results were obtained for aging at 250 °C for 15 min. Volumetric shrinkage occurred during aging at both 175 and 250 °C due to the differences in the diffusion rates between the Al and Au atoms, thus promoting the growth of creep cavities at the void line [175].

In a study on the effects of high temperature on bond degradation, Teverovsky [176] studied Au–Al wire bonds in plastic-encapsulated microcircuits (PEMs) in vacuum conditions. Three groups of linear devices—dual-operational amplifier (OP) and two types of precision band gap voltage reference microcircuits, referred to as LT and AD—were subjected to HTS in convection air chambers and in a vacuum chamber. The electrical characteristics of the devices, variations in the wire bond contact resistances, mass losses of the packages, and thermo-mechanical characteristics of the molding compounds were recorded. The results showed that the thermo-mechanical characteristics of molding compounds under HTS in both the vacuum and air conditions were similar.

Fig. 5.1 Distributions of contact resistance of wire bonds in precision band gap voltage reference (AD) parts at 210 °C for different exposure times (in hours) in (a) air and (b) vacuum [176]



The failure rate and degree of wire bond degradation for parts stored in air, however, were higher than those for parts stored in the vacuum chamber, as seen in Figs. 5.1, 5.2, and 5.3. Figure 5.1 shows a comparison of the distributions of the contact resistance of wire bonds in precision band gap voltage reference (AD) parts at 210 °C in air and vacuum conditions. It can be seen that the scatter of contact resistance (RC) is less in the parts in a vacuum than in the parts in air. Similarly, the variations of contact resistances for LT and OP parts are smaller for parts in a vacuum than for parts kept in air, as shown in Fig. 5.2. Figure 5.3 shows that the cumulative probability of wire bond failures in both OP and LT parts is lower in the parts stored in vacuum chambers than in the ones stored in air.

For PEMs, the degradation process is governed by the mechanical stresses in the package and the release of corrosive molecules from the mold compound (MC). Thermal decomposition of the epoxy materials in MCs and flame-retardant additives forms multiple chemically active molecules such as methyl bromide (H3C-Br), hydrogen bromide (HBr), water, and carbon oxides. These molecules can react with Au-Al intermetallics, causing dry corrosion of the bond [176].

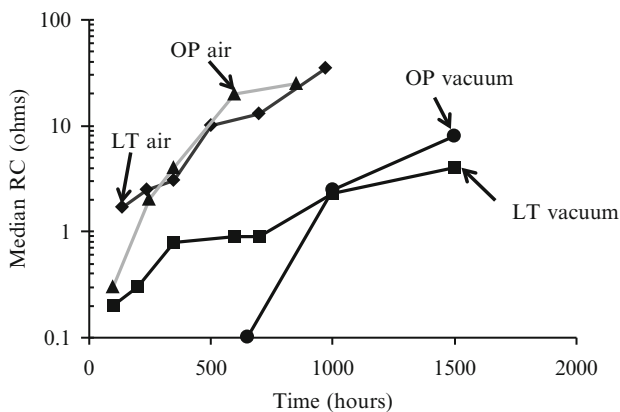


Fig. 5.2 Kinetics of contact resistance variations during air and vacuum storage for dual-operational amplifier (OP) and precision band gap voltage reference (LT) microcircuits [176]

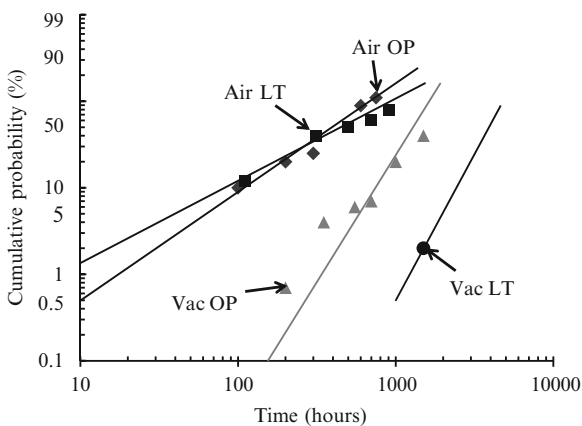


Fig. 5.3 Cumulative probability for wire bond failures ($RC > 10 \Omega$) during storage of OP and LT parts in air and vacuum chambers [176]

5.1.2 Bare Cu on Al, Au, and NiPdAu Pads

Leong et al. [119] investigated Cu bonding on direct immersion gold (DIG) finish and found that Cu bonds on Au bond pads passed qualification tests and had good reliability. Figure 5.4 shows the package used for qualification testing with Cu-Ni/Au pads.

The Cu wire thickness was $20 \mu\text{m}$ and the immersion Au thickness was $0.3 \mu\text{m}$ for the die pad. The lead fingers had a surface finish of electrolytic gold with $0.5 \mu\text{m}$ thickness. The bonding parameters are listed in Table 5.1.

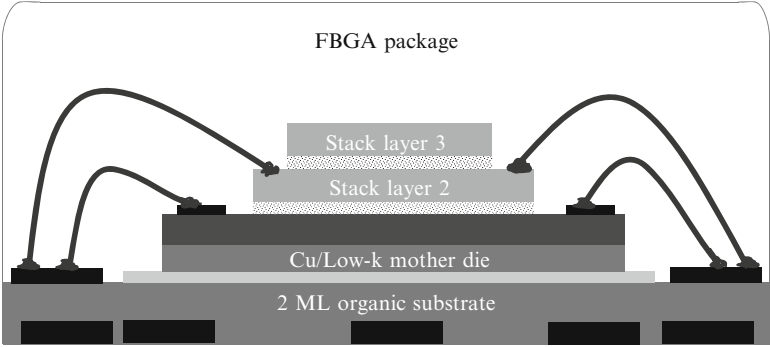


Fig. 5.4 Cross-sectional view of FBGA package [119]

Table 5.1 Bonding parameters for bare Cu on Au pad [119]

Bonding Parameters	Ball Bond	Wedge Bond
Contact time (ms)	2	3
Contact power (mW)	2.5	0
Contact force (N)	0.235	0.392
Base time (ms)	10	15
Base power (mW)	39	138
Base force (N)	0.118	0.343

Package-level reliability tests were conducted for 1,000 h, and no failures were observed. The study found that the package passed qualification testing as long as Cu was prevented from oxidizing. Test targets were set to be a minimum of 0.029 N for pull strength and a minimum of 0.078 N for ball shear strength [119]. Bonds formed by Cu wire on Au pads passed the reliability tests with pull strength and shear strength values above the target test specifications. They also passed the thermal cycling (−40 °C/125 °C) qualification test requirements of 1,000 cycles.

HTS testing was conducted at 150 °C for 1,000 h, after which time the pull and shear tests were carried out [119]. Wire pull and ball shear tests were carried out after HTS (150 °C) up to 1,000 h. All the bonding connections exhibited the required strength, and no obvious degradation was observed. Figures 5.5, 5.6, and 5.7 show the results of the ball pull tests, shear tests, and wedge pull tests, respectively, at time zero and after HTS aging for 250, 500, and 1,000 h at 150 °C. Pull strength was in the range of 0.078–0.118 N (Fig. 5.5), where the pull strength had a target specification of greater than 0.029 N. Shear force for the first bond was in the range 0.196–0.343 N (shear force target > 0.078 N) (Fig. 5.6); and wedge pull strength values were in the range of 0.049–0.078 N (Fig. 5.7).

Ratchev et al. [154] compared the bonding strength of Cu wire to Au wire on NiPdAu (5 μm/500 nm/80 nm) and NiAu (3 μm/80 nm) pads under shear tests and found that Cu wire had a higher bonding strength than Au wire (Fig. 5.8). The higher strength of Cu wire is due to the higher stiffness of Cu wire compared to

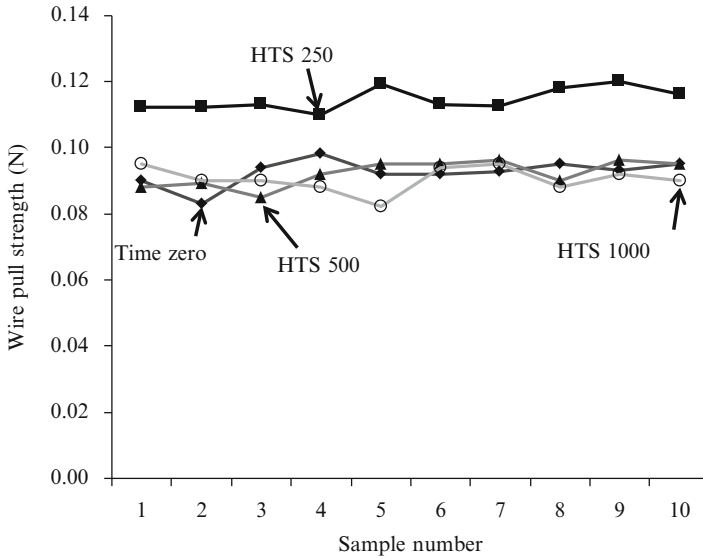


Fig. 5.5 Wire pull readings at different HTS intervals (20 μ m Cu wire) [119]

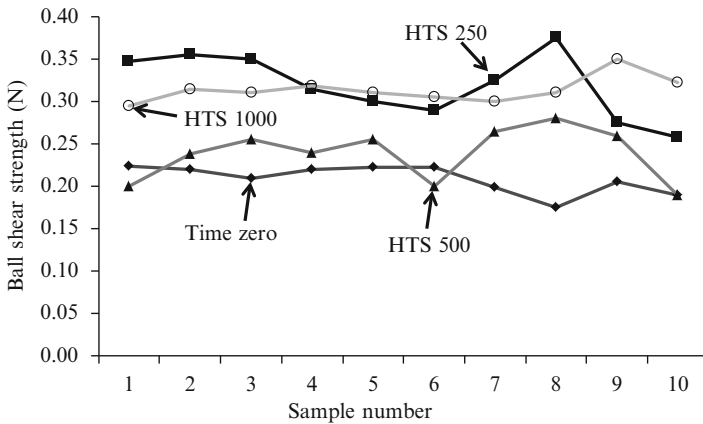


Fig. 5.6 Ball shear readings at different HTS intervals (20 μ m Cu wire) [119]

Au wire. It was also found that Cu on Ni-based pads had higher pull strength than the Cu–Al interface.

Figure 5.9 shows the fracture mode of several pad finishes for Cu and Au wire bonds under shear tests. The fracture mode for Au was found within the ball, whereas for Cu it was mostly on the bond pad [154].

Clauberg et al. [23] examined the shear strength of Cu wire (20 μ m thick) bonds on 1 μ m Al pads plated with NiPd and NiPdAu finishes of varying thicknesses (samples A–H in Table 5.2). The assemblies were subjected to 175 $^{\circ}$ C for 1,000 h, and a shear

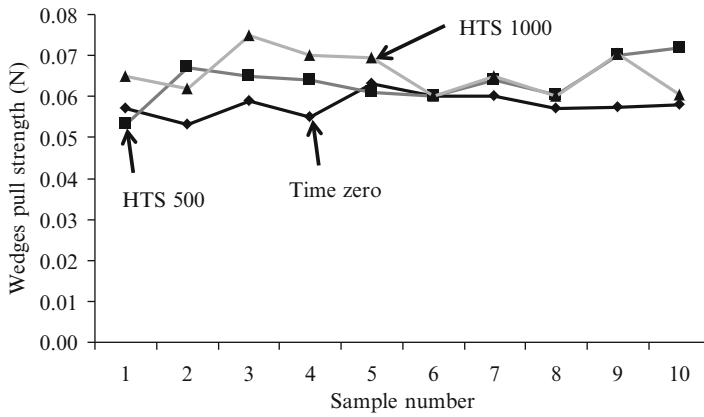


Fig. 5.7 Wedge bond pull readings at different HTS intervals (20 μm Cu wire) [119]

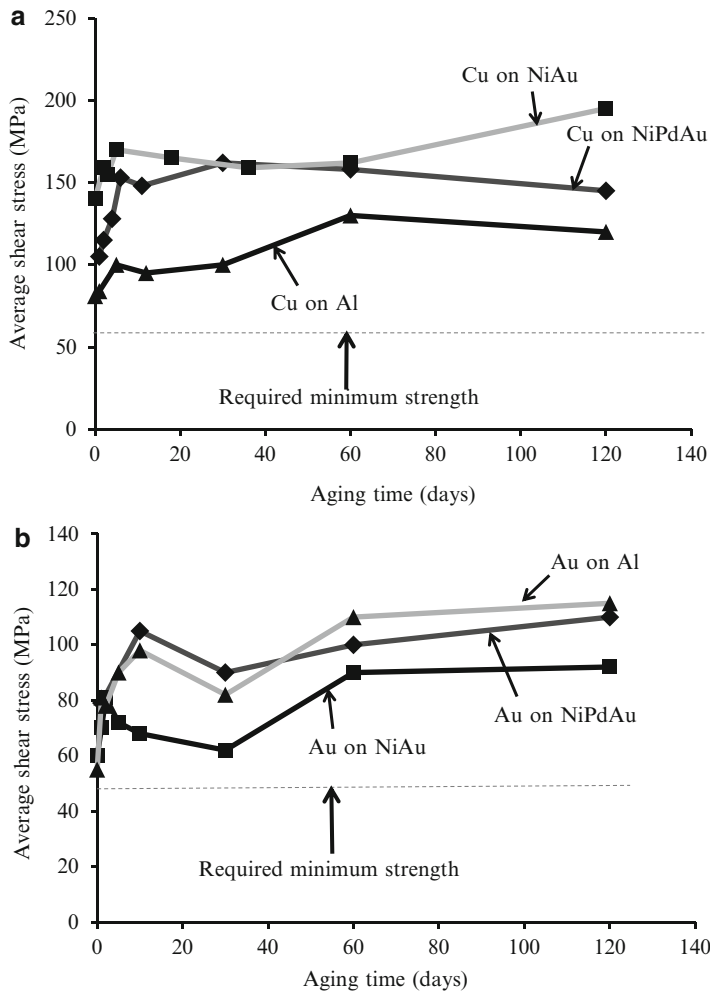


Fig. 5.8 Shear strength of (a) Cu and (b) Au wire on different pad metallurgies (aged at 150 $^{\circ}\text{C}$) [154]

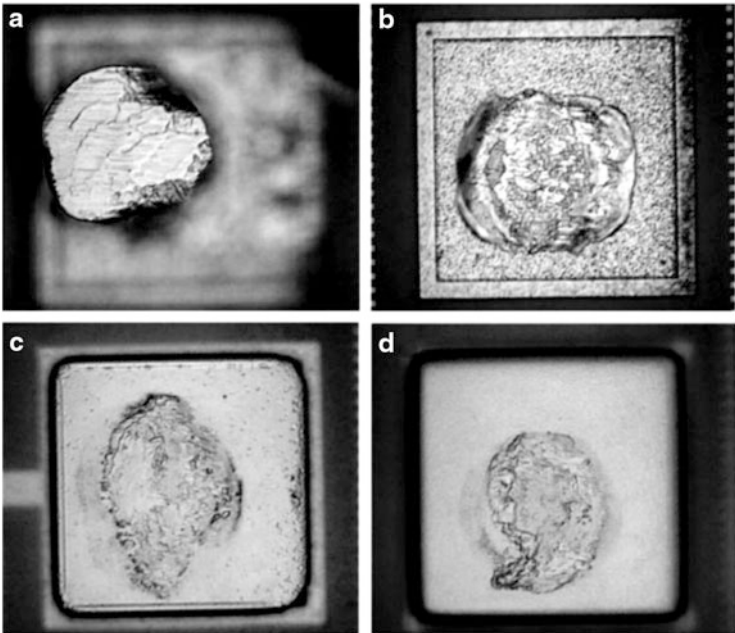


Fig. 5.9 Fracture mode in shear tests: (a) Au wire on Al pad; (b) Cu wire on Al pad; (c) Cu wire on Ni–Au pad; (d) Cu wire on NiPdAu pad [154]

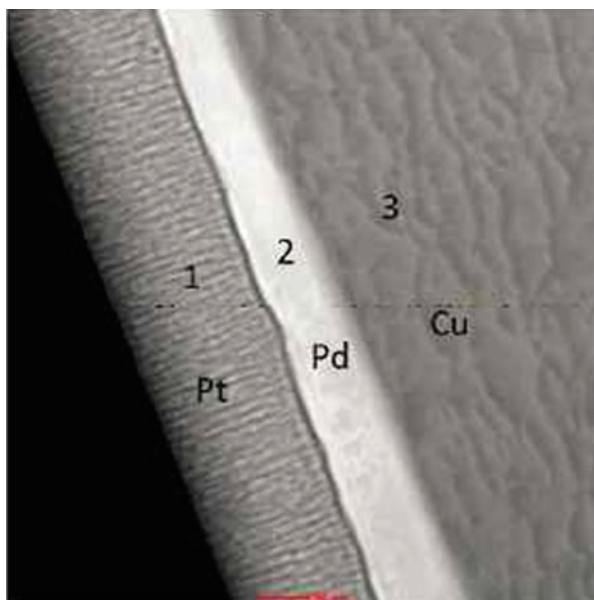
Table 5.2 Shear strength for 20 μm Cu wire [23]

Sample type	Ni (μm)	Pd (μm)	Au (μm)	XY Avg (μm)	Ball height (μm)	Shear strength (N)	Shear/area ($\mu\text{N}/\mu\text{m}^2$)
Control	1 μm Al, control die			39.4	8.1	0.147	120.12
A	3	0.3	0.03	39.2	9.2	0.241	200.71
B	3	0.3	0	39.5	9.4	0.254	206.80
C	3	0.1	0.03	39.1	9.3	0.238	199.19
D	1	0.1	0	39.3	8.8	0.240	197.67
E	1	0.1	0.03	39.5	8.9	0.252	205.28
F	1	0.3	0.03	39.3	8.4	0.254	209.84
G	3	0.1	0	39.2	9.2	0.255	211.36
H	1	0.3	0	39.3	8.4	0.245	202.23

test was carried out. The results (Table 5.2) indicated more than a 50 % higher shear strength for bonds on NiPdAu pads compared to control Al pads. No trend was observed with the varying thickness combinations of NiPdAu metallurgies.

The shear failure mode was different for NiPdAu pads than for the Al pad [23]. For Cu–Al bonds, shear failure was found either at the Cu–Al interface or within the Al, indicating a weak Cu–Al interface compared to the Cu ball. However, contrary to the findings of Ratchev et al. [154], Clauberg et al. [23] found that for NiPdAu

Fig. 5.10 TEM image showing a Pd layer on Cu [51]



metallurgies, shear failure was a typical failure mode through the Cu ball, indicating that the Cu–Pd interface is a stronger interface than Cu–Al.

5.1.3 Bare Cu vs. Palladium-Coated Copper Wires

Cu and PdCu wires have been compared under HTS tests [49, 51]. Qin et al. [51] compared Cu and PdCu wire bond strength using 18 μm Cu and PdCu wire with bonded ball diameters of about 33 μm on aluminum pads. The thickness of the Pd layer was around 80 nm, and first (ball) and second bonds were examined for pull strength.

First bond comparisons of Cu and PdCu wires for un-aged (as-bonded) samples showed that the PdCu wire had about 11 % higher pull strength than the Cu wire [51] (see A.5 and A.6), indicating that the PdCu wire had a higher tensile strength. Pull strength comparisons were also made for the first bonds after high-temperature aging at 175 °C for up to 168 h. It was found that the bond strength for PdCu wire degraded after just 24 h at 175 °C, also leading to a higher rate of pad peeling failure than is found in Cu. The results indicated that the cause of bond pull strength degradation was the congregation of Pd near the interface, where over 65 % of PdCu bonds peeled off and only ~5 % Cu bonds failed. Interfacial metallurgies were analyzed on PdCu wire and ball bonds using high-resolution transmission electron microscopy (HRTEM), along with energy-dispersive X-ray spectrometer (EDX). Figure 5.10 shows the results of TEM scans of the PdCu wire, where the locations of Cu and Pd can be seen. The numbers 1, 2, and 3 indicate the locations of the TEM scan. The Pt layer is from the TEM sample preparation [51].

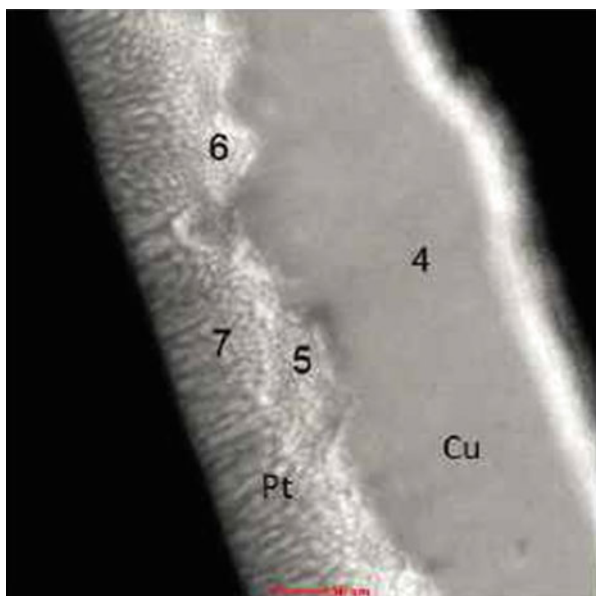


Fig. 5.11 TEM image showing the absence of a Pd layer after bonding (no aging) [51]

Figure 5.11 shows the results of TEM scans on the PdCu ball bonds in locations 4, 5, 6, and 7. A Pd layer was not found in the scan results, since after bonding most of the Pd dissolved into the Cu.

The interfacial metallurgy for PdCu wires was analyzed after high-temperature aging (Fig. 5.12a, b). The line 1 in Fig. 5.12a shows the region where the EDX scans were conducted, with numbers 1–6 indicating the exact locations of EDX scans. Figure 5.12b shows the results of the line scans, and the locations of Pd, Cu, and Al can be seen. It was found that after high-temperature aging, Pd congregated and diffused back to the interface.

A comparison of second bonds was conducted for Cu and PdCu wires on a BGA substrate. The stitch pull strengths were similar, but PdCu showed 50 % higher tail pull strength than Cu bonds [51].

Uno et al. [49] also examined the initial stitch pull strength of bare Cu and PdCu wires after various storage durations. The first bond was on pure Al pads that were 1 μm thick, while the second bonding process, stitch bonding, was conducted on silver-plated lead frames. Figure 5.13 shows the results of the stitch pull strength comparisons of bare Cu wire and PdCu (EX1) wire.

Nonstick-on-lead (NSOL) was observed for the PdCu (EX1) wire, whereas the bare Cu wire exhibited NSOL of ≥ 1 %. It was found that PdCu wire showed higher pull strength than bare copper wire. Pd-coated Cu wire maintained a high pull strength for up to 90-day storage in air, while bare Cu wire severely deteriorated within the first 7 days [49].

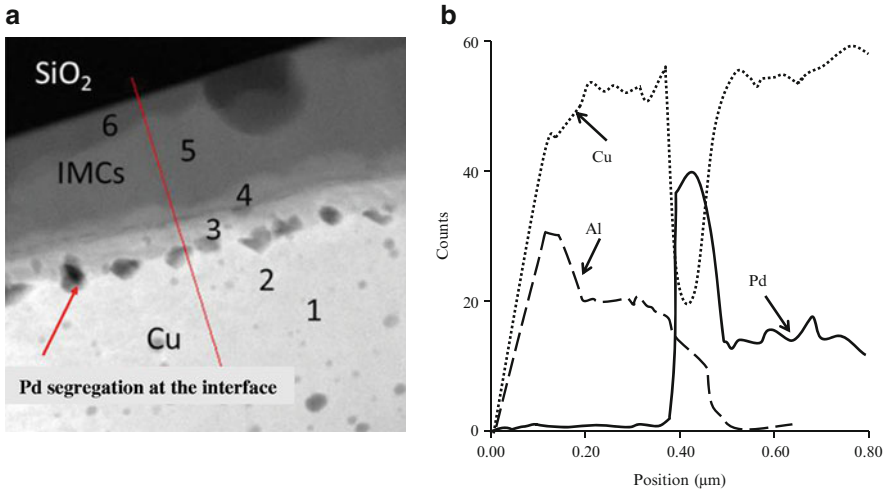


Fig. 5.12 EDX spectra indicating the presence of Pd at the bonding interface after aging at 175 °C for 24 h [51]

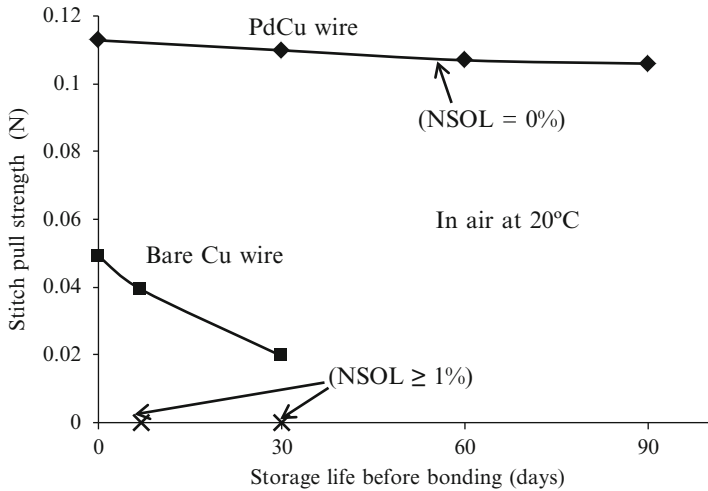
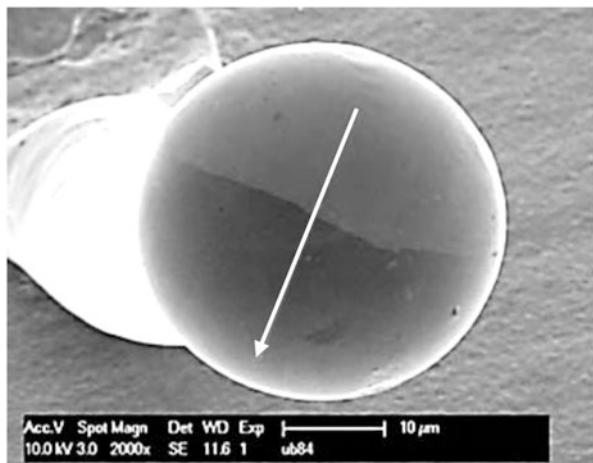


Fig. 5.13 Stitch pull strength vs. storage time of PdCu (EX1) wire in air before bonding [49]

Stephan et al. [58] conducted HTS testing at 175 °C for 2,000 h and ball shear and pull tests. PdCu showed higher pull and shear strengths than bare Cu and showed no degradation during the entire test period. However, interface analysis revealed that there was no major difference in the phase formation and IMC thickness for PdCu and bare Cu bonding.

Fig. 5.14 Pd distribution in an FAB formed with PdCu wire [120]. Moving along the line from top to bottom the Pd concentration increases as the image gets darker



Zhang et al. [120] compared the first and second bond strengths of pure copper wire and PdCu wire under shear and tensile tests. The diameters of both wires were 25 μm , and the thickness of the Pd coating was approximately 100 nm. It was found that PdCu wires had lower shear bond strengths at the first bonds than the pure Cu wire. A tensile stress comparison for the second bonds of two wire types after aging at 180 $^{\circ}\text{C}$ for 16 h was conducted to examine the oxidation-resistant properties of Pd. The results indicated that PdCu wire had higher tensile bond strength at the second bonds than pure Cu wire.

As of 2013, the role of Pd in the reliability of Cu wire is not fully understood. However, studies have indicated that the distribution of Pd might impact bond reliability. Many studies have reported that PdCu wire shows better performance than bare Cu wire and gold wire on Al pads [50, 58, 166, 177]. Since Pd does not participate in IMC formation, the presence of a Pd layer is not expected to influence bondability. However, Pd segregates at the interface after extended aging at high temperatures. For example, Lu et al. [178] reported segregation of Pd at the interface after aging at 250 $^{\circ}\text{C}$ for 3 h, which might influence the bond strength.

The distribution of Pd in a free air ball (FAB) affects the Pd distribution at the bonding interface. Tang et al. [92] investigated Pd distribution in the FAB and wire region, and reported that the Pd layer is thicker at the wire neck and gradually thins down towards the FAB diameter. Pd was thinnest at the hemisphere near the tip of the FAB. Zhang et al. [120] reported that Pd distribution at the bonding interface can be determined by the wire tail's shape. A flat-headed wire tail leads to symmetrical distribution of Pd. A wedge shape causes asymmetrical distribution of Pd on an FAB, which can lead to the presence of Pd in part of the bonding interface. Figure 5.14 shows the asymmetry in the distribution of Pd on FABs in PdCu wire. The light gray area shows a higher Pd content than the darker area, and the PdCu reduces gradually along the line in Fig. 5.14 (4.87 to 4.62 to 1.15 to 0.34 to 0.07 at.%).

Kumar et al. [109] have also reported that, after FAB formation, Pd distribution was not uniform on the FAB. In contrast, some studies have reported that a uniform

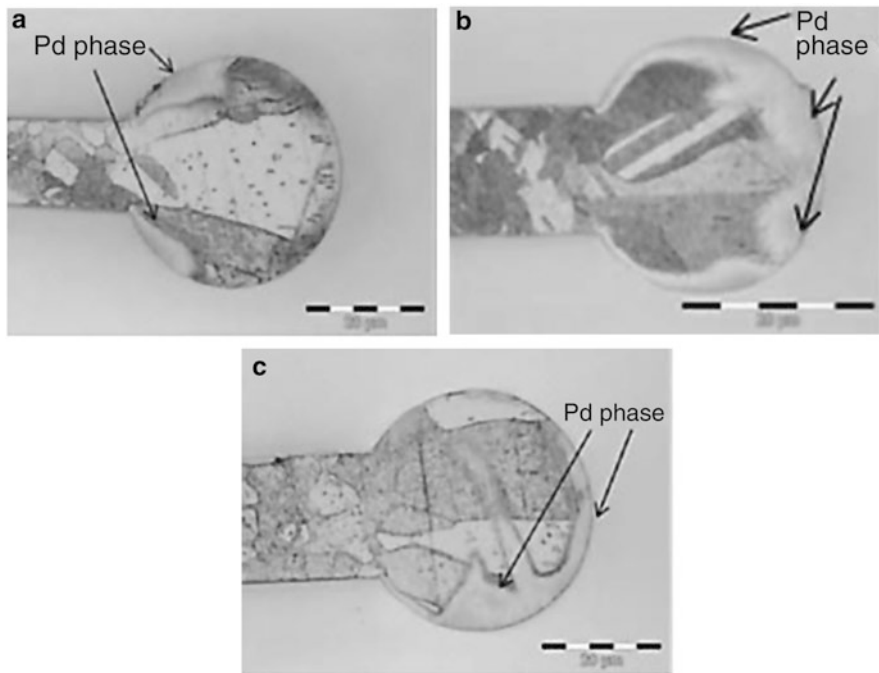


Fig. 5.15 Pd distribution in FABs at (a) 30 mA; (b) 60 mA; (c) 120 mA EFO current [93]

Pd layer around an FAB can be achieved. Tang et al. [88] suggested using a high electrical flame-off (EFO) current (90 mA for 20 μm PdCu wire) to obtain a uniform layer (~ 14 nm thickness) around the FAB.

Clauberg et al. [93], however, found that a higher EFO current leads to a more random Pd distribution on the FAB, because the higher temperature caused by the higher current makes Pd dissolution into the Cu ball easier (Fig. 5.15).

Ching et al. [179] reported that the distribution of Pd can be controlled in a forming gas environment better than in a nitrogen environment. Techniques such as SEM, EDX, and planar cut FIB [53, 180] are used to investigate the Pd distribution in the FAB and at the bond–pad interface. Systematic research should be conducted on how Pd moves within the bonds and interacts with Cu and the pad metal.

5.1.4 IMC Growth Model and Acceleration Factor

Wire bond degradation in HTS tests is mainly related to the bond–pad interface degradation. The growth of interfacial IMC at the bonding wire–pad interface is an indicator of bond wire–pad interface degradation. IMC growth under different

Table 5.3 Activation energies and reaction rates of Cu–Al IMC growth

IMC	HTS temperature (°C)	E_a (kJ/mol)	K_o (m ² s ⁻¹)	References
CuAl	175, 200, 250	60.79	1.21×10^{-7}	[121, 124]
CuAl	200, 250, 300	97.45	1.21×10^{-7}	[126]
CuAl	150, 200	129.29	1.63×10^{-4}	[181]
CuAl	175, 200, 225, 250	121.57	3.70×10^{-5}	[129]
CuAl	150, 180, 200	121.57	Unknown	[182]
CuAl	150, 250, 300	109.99	1.39×10^{-8}	[183, 123]
CuAl	150, 175, 200	113.85	1.43×10^{-8}	[184]
CuAl	150, 200, 250	44.38	1.64×10^{-6}	[185]
AuAl	150, 175, 200	100.35	1.97×10^{-9}	[184]

HTS test conditions can be used to obtain the corresponding acceleration factors. The IMC growth model is given by the Arrhenius equation as follows:

$$X^2 = K \times t \quad (5.1)$$

where X is the IMC thickness (in cm) at time t (in seconds), and K is the reaction rate in cm²/s given as follows:

$$K = K_0 \times e^{\left(-\frac{Q}{RT}\right)} \quad (5.2)$$

where Q is the activation energy in kJ/mol, R is the gas constant in kJ/Kmol, and T is the temperature (in Kelvin). Cu–Al growth model can be generated by obtaining the reaction rate (K) and activation energy (Q) from the IMC thickness data at different temperature and time. The obtained growth equation is given by

$$X^2 = t \times K_o \times e^{\frac{-Q}{RT}} \quad (5.3)$$

Using (5.3), the higher temperature at a shorter aging time can be related to the lower temperature at longer aging times. The above equation can also be used to predict the IMC thickness at a given aging temperature and time. Table 5.3 shows the activation energy and reaction rate values for the CuAl system as reported in the literature.

The acceleration factor for CuAl IMC growth at temperature T_1 and T_2 ($T_1 > T_2$) is given by

$$X_1 = \sqrt{t \times K_o \times e^{\frac{-Q}{RT_1}}}$$

$$X_2 = \sqrt{t \times K_o \times e^{\frac{-Q}{RT_2}}}$$

$$AF = \frac{X_1}{X_2}$$

$$AF = e^{\frac{\sigma}{2\pi} \left(\frac{1}{r_1} - \frac{1}{r_2} \right)}$$

The acceleration factor of IMC growth can be related to the bond interface degradation, and correlations can be made with the wire bond strength and reliability.

5.2 Thermal Shock and Thermal Cycling Tests

Temperature cycling can precipitate failure due to flexure resulting from differences in thermal expansion of packaging materials including die attach, mold compound, encapsulants, and PCB/substrate. The failure mechanisms addressed by the test include flexure failure of the wire at the heel, bond pad–substrate shear failure, and wire–substrate shear failure [186]. These failure mechanisms can be activated by excessive neck down at the heel, excessive embrittlement of the wire during bonding, and poor bond shear strength resulting from surface roughness and the presence of contaminants.

Three main stresses undergone by the wire during thermal cycling are flexural, axial, and shear [187]. They are described below.

Wire Flexure

The cyclic amplitude of bending stress at the heel of the wire due to thermal expansion during temperature cycle is given by the theory of curved beams and the simple theory of linear elasticity [188]:

$$\varepsilon = 6 \left(\frac{r}{D} \right) \left(\frac{L}{D} - 1 \right)^{0.5} \left[2\alpha_{\text{base}} + \frac{\alpha_{\text{base}} - \alpha_{\text{wire}}}{1 - (D/L)} \right] \Delta T$$

where r is the wire radius, α is the coefficient of thermal expansion, L is the wire length, D is the span between the bonds at the two ends of the wire, and ΔT is the change in temperature during temperature cycling. The above formulation assumes that the bond pads are at the same height.

The cycles to failure in flexure are given by Coffin–Manson model:

$$N_f = C\varepsilon^m$$

where C and m are determined empirically.

Wire encapsulated in the mold compound experiences axial stress due to the difference in expansion rates between the mold compound (e) and the wire (w). The stress in the wire is given by

$$\sigma_w = E_w(\alpha_e - \alpha_w)\Delta T$$

where α is the coefficient of thermal expansion, E is the modulus, and ΔT is the change in temperature during temperature cycling.

Again, the cycles to failure are given by Coffin–Manson model for low-cycle fatigue:

$$N_f = C\sigma^m$$

Shear of the Bond Pad

The shear stress distribution in the pad is given by [188]

$$\tau = \frac{G_p \Delta T}{b_p Z} \left\{ (\alpha_w - \alpha_s) - \frac{(\alpha_s - \alpha_p)}{1 + (E_s A_s) / [E_p A_p (1 - \nu_s)]} \right\} \frac{\sinh(Zx)}{\cosh(Zl_w)}$$

$$Z^2 = \frac{G_p}{b_p} \left[\frac{r}{E_w A_w} + \frac{(1 - \nu_s) W_p}{E_s A_s} \right]$$

The amplitude of the maximum shear stress due to the temperature cycle ΔT at the critical point $x = l_w$ is given by

$$\tau_{\max} = Q \Delta T$$

$$Q = \frac{G_p}{b_p Z} \left[(\alpha_w - \alpha_s) + \frac{(\alpha_s - \alpha_p)}{1 + (E_s A_s) / [E_p A_p (1 - \nu_s)]} \right]$$

The number of cycles to failure of the bond pad material is given by

$$N_f = C'_p \tau_{\max}^{-m'_p}$$

where C'_p and m'_p are determined empirically.

Shear of Wire and Substrate

Maximum shear stresses in the wire (w) and substrate (s) are given by [188]

$$\tau_{w,\max} = \left\{ \frac{r^2}{4Z^2 A_w^2} \left[\frac{\cosh(Zx_w)}{\cosh(Zl_w)} - 1 \right]^2 + \frac{Q^2 \sinh^2(Zx_w)}{\cosh^2(Zl_w)} \right\}^{\frac{1}{2}} \Delta T$$

$$\tau_{s,\max} = \left\{ \left[\frac{W_p Q}{2Z A_s} \left(1 - \frac{\cosh(Zx_s)}{\cosh(Zl_s)} \right) + \frac{(\alpha_s - \alpha_p)}{(1 + \nu_s)/(E_s) + A_s/(E_p A_p)} \right] \right. \\ \left. + Q^2 \frac{\sinh^2(Zx_s)}{\cosh^2(Zl_s)} \right\}^{\frac{1}{2}} \Delta T$$

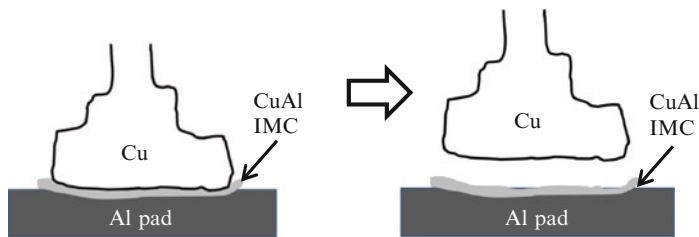


Fig. 5.16 Failure under thermal cycling loading

where r is the wire radius, A is the cross-sectional area, W is the width, G is the shear modulus, b is the thickness, l is the length of the wire, ν is the Poisson's ratio, and Z is the Eigen value expressed in terms of material properties and geometry of the wire bond assembly:

$$x_w = \tanh\left(\frac{A_w}{r_w}\right), \quad x_s = \tanh\left(\frac{A_s}{r_s}\right), \quad A_s = b_s(w_s + w_p)/2$$

The numbers of cycles to shear fatigue failure of wire and substrate material are given by Coffin–Manson equation for high-cycle fatigue as follows:

$$N_f = C'_w \tau_{\max}^{-m'_w}$$

$$N_f = C'_s \tau_{\max}^{-m'_s}$$

where C'_w , m'_w , C'_s and m'_s are the experimentally determined shear fatigue properties for the wire and substrate materials.

5.2.1 Bare Cu and PdCu Wires

Wire bond failures under thermal cycling tests have been mainly observed at the bond–pad interface. Due to CTE mismatches between Cu wire (17 ppm/°C), Al pad (24 ppm/°C), and Si die (3 ppm/°C), the bond–pad interface is under stress during temperature cycles. Additionally, interfacial Cu–Al IMC continues to grow under temperature cycling, and micro-cracking may occur at the interface. Gan et al. [189] illustrated the mechanism of wire bond failures as follows (Fig. 5.16): the CTE mismatch between the Cu ball and the underlying Al pad results in differential expansion and contraction at the interface. The Cu–Al IMC experiences strain and starts to crack as the thermal cycling progresses. Repeated thermal cycling stresses result in bond pad separation, resulting in failure.

Cu wire-bonded packages have been qualified under thermal cycling tests [57, 119, 190]. In a study conducted by Tian et al. [99], small outline transistor (SOT) devices interconnected with 20 μ m copper wire and encapsulated with commercial

Table 5.4 Comparison of TC reliability of PdCu and Au wires [184]

Wire	Test	Test condition	t_{first} (h)	t_{50}	$t_{63.2} (\eta)$	β
PdCu	TC	−40 to 150 °C	7,000	12,544	13,301	5.79
Au	TC	−40 to 150 °C	6,000	11,982	12,922	4.72

epoxy molding compound (EMC) were subjected to thermal shock tests. The copper balls were bonded on an Al pad with 3 μm thickness, and the wedge bonds were bonded on silver (Ag)-plated lead-frame fingers. The temperature range was from −50 to 150 °C, the ramp rate was 20 °C/min, and the dwell time at each temperature extreme was 10 min. The cycle duration was 0.5 h. The results showed that no voids or cracks were observed up to 1,500 cycles of the thermal shock test. Also, all the SOT devices passed the electrical operation examination for up to 1,500 cycles. The high thermal shock resistance was attributed to the low Cu–Al IMC growth rate.

Leong et al. [119] reported that molded Cu wire bond packages passed 1,000 cycles of −40 to 125 °C, qualified by electrical tests. Another study by Anh et al. [57] indicated that electrical test results for 176 low-profile quad flat packages (LQFPs) after 1,000 air-to-air temperature cycling cycles (−65 to 150 °C) showed no failures for both Cu wire on Al pads and Cu wire on NiPdAu pads.

Recently, Gan et al. [184] compared the thermal cycling reliability of 20 μm PdCu wire and 4 N Au wire. The thermal cycling profile was −40 to 150 °C. It was found that PdCu wires exhibited better thermal cycling performance than Au wire, as shown in Table 5.4.

5.2.2 Failure Model and Acceleration Factor for Thermal Cycling Tests

In this section, guidelines for obtaining the AF for thermal cycling tests are provided. The Coffin–Manson model is used to estimate time to failure in thermal cycling tests. The simplified model is

$$N_f = A(\Delta T)^n$$

where N_f is the time to failure, A is constant for a given material system, ΔT is the difference between the maximum and minimum temperature in the thermal cycling test, and n is the model constant. The acceleration factor for a thermal cycling test under ΔT_1 and ΔT_2 is given as follows:

$$N_{1f} = A(\Delta T_1)^n$$

$$N_{2f} = A(\Delta T_2)^n$$

$$AF = \frac{N_{1f}}{N_{2f}}, \quad \text{where } N_{1f} > N_{2f}$$

5.3 Summary

Thermal stress tests, including HTS, thermal cycling, and thermal shock tests, are carried out to evaluate the strengths of Cu wire bonds. Evaluation of the bondability and reliability of copper wire bonding considers both as-bonded reliability and long-term reliability. HTS tests are conducted to accelerate interfacial IMC growth at the wire bond–bond pad interface and then determine its effect on wire bond strength.

Shear and pull tests are conducted after temperature cycling, shock, and humidity tests. Researchers have reported that the bonding strength of Cu wire on NiPdAu and NiAu pads under pull and shear tests is higher than that of Au wire. The higher strength of Cu wire is due to the higher stiffness of Cu wire than Au wire. Comparisons of the first bonds of Cu and PdCu wires for as-bonded samples indicate that PdCu wire has a higher pull strength than Cu wire. However, the bond strength for PdCu wire degrades after just 24 h at 175 °C, also leading to a higher rate of pad peeling failure than Cu. The cause of bond pull strength degradation is the congregation of Pd near the interface after extended aging at high temperatures. Comparisons of the second bonds of Cu and PdCu wires on the BGA substrate show that the stitch pull strengths are similar, but PdCu has 50 % higher tail pull strength than Cu.

Temperature cycling is conducted to evaluate the reliability implications of flexure resulting from differences in the coefficient of thermal expansion of the packaging material. The failure mechanisms include flexure failure of the wire at the heel, bond pad–substrate shear failure, and wire–substrate shear failure. Cu wire-bonded packages have been qualified against thermal cycling testing and have been shown to pass different temperature cycling test regimes, including –50 to 150 °C, –40 to 125 °C, and –65 to 150 °C for up to 1,000 cycles.

The combined effect of temperature and humidity on wire bond strength is estimated using a pressure cooker test (PCT) and a highly accelerated temperature and humidity stress test (HAST). A PCT, also known as an autoclave test, assesses the reliability of wire bonds in high-temperature and high-humidity environments by aging under saturated pressurized vapor. The JEDEC PCT test conditions are 121 °C and 100 % relative humidity (RH). bHAST is usually carried out at 130 °C and 85 % RH with an applied bias (3.6 V). The bias is applied to accelerate failure. The JEDEC test conditions for an unbiased HAST (uHAST) test are 130 °C and 85 % RH. The failure mechanism addressed by these tests is corrosion of the wire-bonded assembly. Electromigration tests are conducted on wire bonds to evaluate the effects of high current densities on bond strength and reliability.

6.1 Humidity-Related Reliability Tests (PCT and HAST)

Under high-humidity conditions, the failure rate is higher in substrate-based packages than in lead frame packages due to the high moisture absorption and halogen content in substrate packages, which promote corrosion more than in lead frame-based packages. Thus, humidity-related reliability tests are usually conducted on substrate-based packages. The tests could be biased or unbiased based on the presence or the absence of voltage stress, respectively. bHAST is a more severe test than uHAST due to the voltage [99, 190, 191]. Gan et al. [192] illustrated the mechanism of wire bond degradation under HAST test (Fig. 6.1). Cu_9Al_4 and CuAl_2 are the major intermetallic compounds (IMCs) formed in a CuAl system.

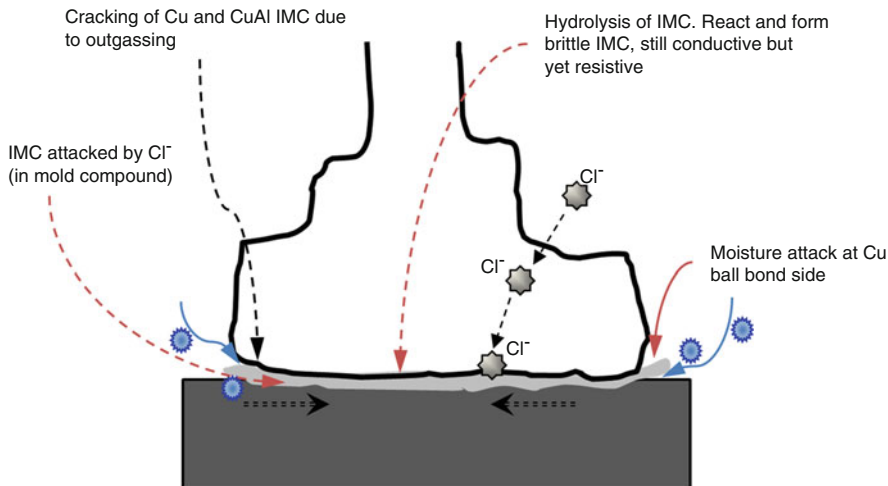
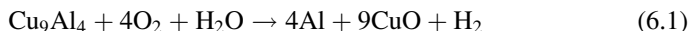
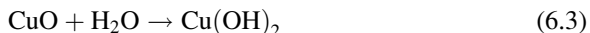


Fig. 6.1 Mechanism of wire bond degradation under HAST test [192]

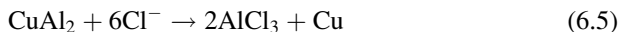
Under HAST conditions, moisture (H_2O) and Cl^- from the mold compound attack these IMCs. Oxygen penetrates from the edge of the ball and induces oxidation of CuAl IMCs (6.1) and (6.2):



CuO is a resistive layer that undergoes oxidation in the HAST test, producing $\text{Cu}(\text{OH})_2$ (6.3), which induces open after the uHAST test:



The main contributor to the Cu wire bond failure under the uHAST test is Cl^- from the mold compound. Cl^- attacks the CuAl IMCs as follows:



Hydrolysis of CuAl IMC and AlCl_3 under a moisture-rich environment forms Al_2O_3 which is a resistive layer that forms at the corroded ball bond (6.6)–(6.8) [184]:

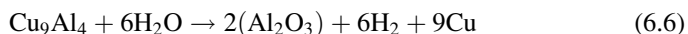
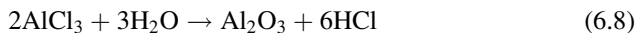
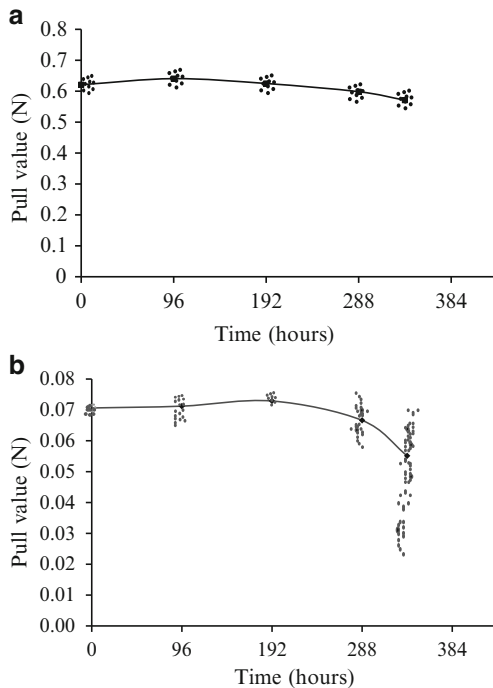


Fig. 6.2 Bonding strength after 336 h of the uHAST in BGA with EMC molding for (a) 20 μm Au wire (forming gas not needed); (b) 20 μm Cu wire (forming gas (5 % H_2 with 95 % N_2) with flow rate of 0.4 l/min) [157]



The outgassing of H_2 during the hydrolysis of CuAl_2 induces cracking at the Cu ball and pad interface. The crack starts at the bond periphery and moves towards the center of the ball. The formed AlCl_3 further hydrolyzes and produces HCl .

6.1.1 Bare Cu Wire

Kim et al. [157] investigated the reliability of 20 μm Au and Cu wires of 4 N purity, bonded on Al pads under HAST conditions of 130 $^\circ\text{C}$ and 85 % humidity. Pull strength tests were conducted after 336 h of the HAST. It was found that Cu wire had a higher pull strength than Au wire under the HAST until 288 h, after which time the pull strength decreased and became lower than that of Au (Fig. 6.2). The low reliability of Cu wire in the HAST after 288 h was attributed to corrosion, which led to crack generation at the Cu–Al interface.

In the above study by Kim et al. [157], the interfacial IMC thickness was found to be 200 nm. No cracks were observed, and the samples met the required minimum

Fig. 6.3 TEM images of the Cu–Al interface: (a) Bond–pad interface that passed pull strength requirements; (b) bond–pad interface with Al oxide layer that failed minimum pull strength requirements [157]

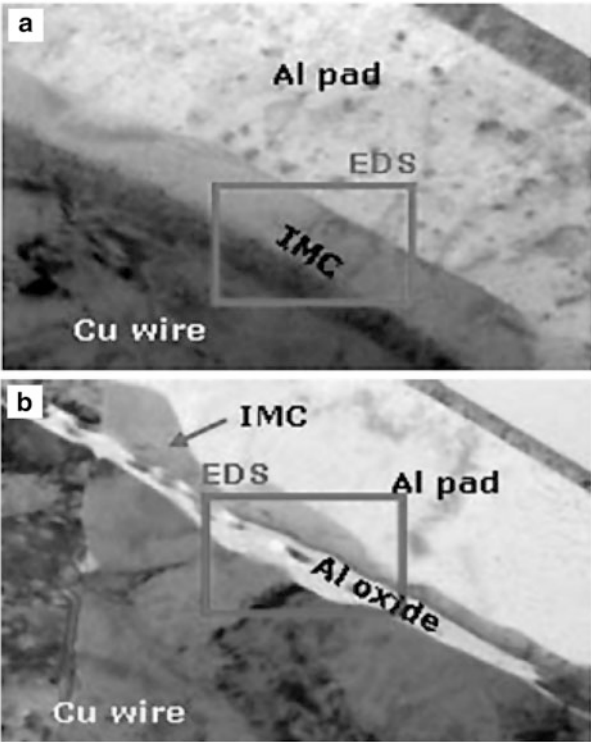


Table 6.1 Potential difference for bonding systems [157]

Metal	Standard reduction potential (Volts)	Potential difference (Volts)	
Au	+1.498	Au–Al	3.16
Cu	+0.337	Cu–Al	1.99
Al	–1.662		

pull strength. The samples that failed to achieve the minimum pull strength had an aluminum oxide layer that caused interfacial degradation (Fig. 6.3).

Corrosion of the Al oxide layer is the reason that Cu–Al systems have low reliability under high-humidity conditions. Corrosion is a galvanic reaction due to the oxidation of aluminum when exposed to moisture. Table 6.1 shows the standard reduction potential of metals. The reduction potential is an indicator of oxidation; a higher number indicates a better oxidizing agent.

In Cu–Al systems, Cu acts as an oxidizing element for Al. On the other hand, although Au is a stronger oxidizing element than Cu, it does not readily react with moisture to form Au²⁺ ions.

Copper oxidation at the interface of the Cu–Al bonding region causes cracks and weakens the Cu–Al bond. Tan et al. [193] studied the corrosion of a Cu–Al system

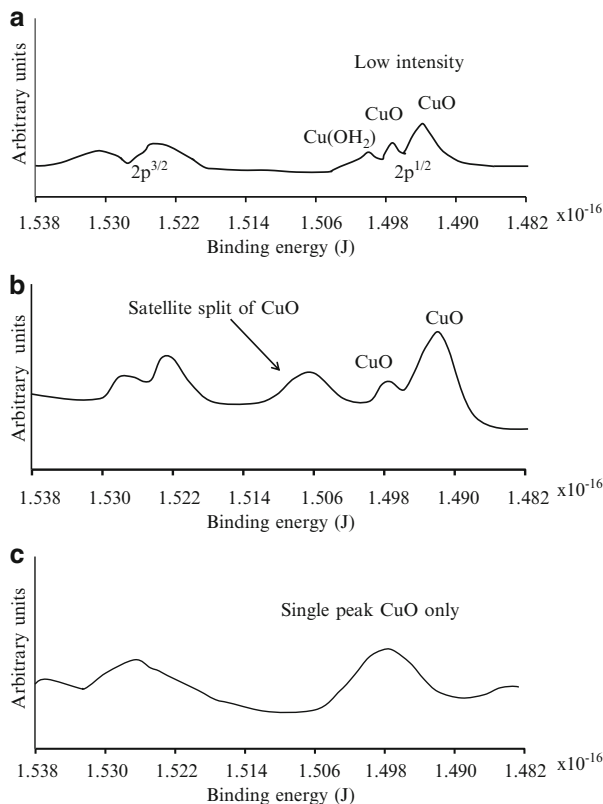


Fig. 6.4 (a) ESCA scan spectra after 0 h of corrosion; (b) ESCA scan spectra after 384 h of corrosion; (c) ESCA scan spectra after 576 h of corrosion [193]

under a PCT (at 120 °C and 100 % relative humidity). The interfacial shear force was examined after the PCT. Surface analysis of the ball-peeled pad with Cu–Al bonding using X-ray photoelectron spectroscopy (XPS) and electron spectroscopy for chemical analysis (ESCA) showed copper oxidation in the Cu–Al interface. Binding energy scans were conducted on the specimen for the 2p photoelectron peaks for Cu after 0, 192, 384, and 576 h in the autoclave test chamber. Figure 6.4a shows the amount of Cu, Cu (OH)₂, and CuO at 0 h of corrosion. As the exposure time increased to 384 h, the amount of Cu decreased and the amount of CuO increased from 0 h (Fig. 6.4b). As shown in Fig. 6.4c, after 576 h of corrosion, no Cu was detected, only CuO. At 0 h, the copper oxide peaks were very low compared to 384 and 576 h. After 576 h of corrosion, the first few atomic layers on the surface changed from Cu to CuO.

Figure 6.5 shows the corrosion rate of a copper specimen as a function of autoclave test time [193]. Initially, there was a higher percentage of Cu (59 %) than CuO (41 %). However, the CuO concentration increased gradually over 384 h

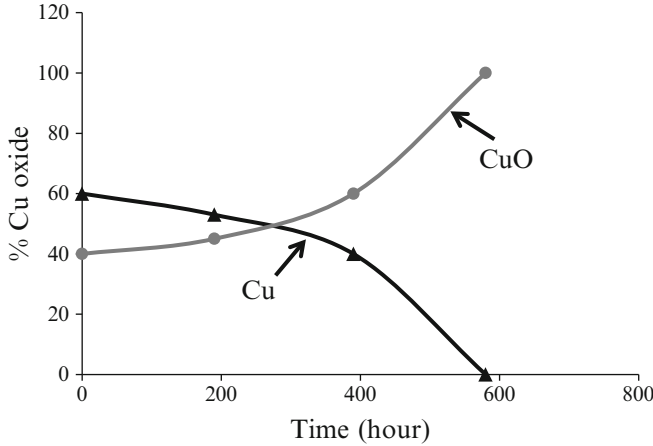


Fig. 6.5 Copper oxide concentration as a function of exposure time [193]

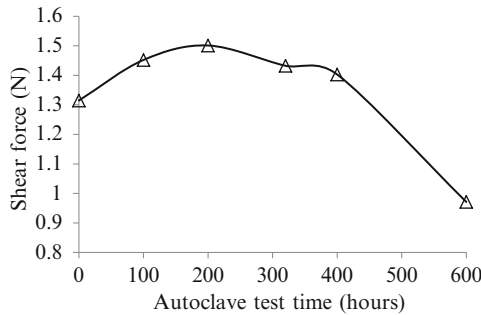


Fig. 6.6 Shear force vs. autoclave test time [193]

under the autoclave test. At 576 h, the Cu turned completely into CuO, with no Cu detected.

Tan et al. [193] examined the corrosion in a copper ball after 0, 288, 384, and 576 h in the autoclave test (at 121 °C and 100 % relative humidity). The Cu–Al interfaces started out visually clean at 0 h. As the autoclave test proceeded, copper oxidation began at the wire region and then spread to the upper bonded area and to the bonding interface. A crack was observed at the Cu–Al interface after 384 h in the autoclave test and eventually led to interfacial failure after 576 h.

The interfacial shear force of copper wire bonding as a function of autoclave test time is shown in Fig. 6.6. There was an initial increase in the interfacial shear force from 1.275 N to 1.540 N after 192 h. However, the interfacial shear force started to decrease after 288 h and reached 0.952 N after 576 h. The Cu–Al bond became weak due to copper oxidation, and the attack decreased rapidly after 384 h in the autoclave test.

6.1.2 PdCu Wire

Kim et al. [157] evaluated the high humidity reliability of 20 μm Pd-coated copper wire. The results indicated that PdCu wire performs better than bare Cu wire on Al pads (Fig. 6.7); however, the presence and distribution of Pd influence the reliability of PdCu wires. The reliability of PdCu wires was compared after 336 h of HAST, where each PdCu wire had a varying concentration of Pd across the ball. When Pd was present on the ball, the surface passed the reliability tests, whereas failures were observed in cases where Pd was present within the balls. The bonding conditions must be considered to minimize Pd diffusion into the ball to achieve high reliability under high-humidity tests.

Tomohiro et al. [194] also evaluated the performance of bare Cu and PdCu wires on Al pads under humidity environments. PCT was conducted at 121 $^{\circ}\text{C}$ and 100 % relative humidity. The results indicated that PdCu wire had greater reliability than bare Cu wire, with a lifetime of 800 h, as compared to 250 h for bare Cu. The bond–pad interface in bare Cu wire showed continuous cracking, possibly due to chlorine (Cl)-induced corrosion, whereas no cracking was observed for the PdCu wire. The high humidity reliability was evaluated using the uHAST. After bonding, the packages were exposed to uHAST conditions of 130 $^{\circ}\text{C}$ and 85 % RH. It was

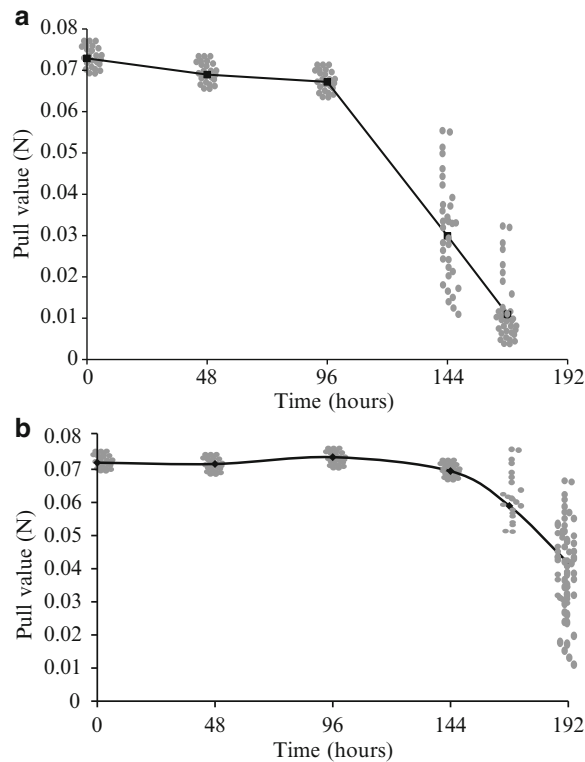


Fig. 6.7 Bonding strength comparison of 20 μm (a) Cu wire and (b) PdCu wire, in BGA packages without EMC molding after HASTs [157]. The forming gas flow rate was 0.5 l/min

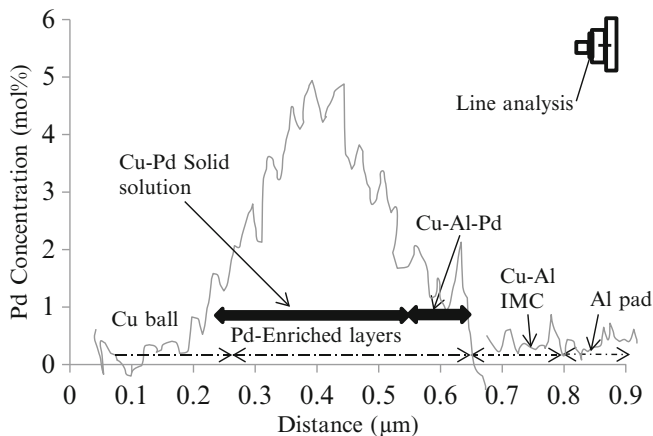


Fig. 6.8 AES line analysis at Cu–Al interface of PdCu wire after PCT for 400 h [194]

found that PdCu wires were more reliable than bare Cu wires. Results also indicated that for PdCu wires, the lifetime under uHASTs was longer than that under PCTs. The PdCu wires had a longer lifetime than the bare Cu wires because of the condensed Pd at the Cu–Al interface due to aging. Figure 6.8 shows the results of auger electron spectroscopy (AES) line scans across the Cu–Al interface. It can be seen that the interface consisted of Pd-enriched layers between the Cu ball and the Cu–Al IMC.

TEM investigation of the Cu–Al interface showed the presence of Pd-enriched layers [194]. The Pd-enriched layers improved the humidity reliability of Cu wire bonds by controlling metal diffusion and IMC formation.

Abe et al. [195] conducted bHAST tests on SOP packages with 20 μm 4 N bare Cu and PdCu wires at 130 °C/85 % RH/3 V. Electrical short/open test was conducted to evaluate the integrity of the package. It was found that PdCu wire shows better humidity than bare Cu wire. They used chemical model simulation technique to predict the IMC creation and the reaction between Cl^- and the IMC. In bare Cu wire, Cu_3Al_2 was corroded by Cl^- from the mold compound. In case of PdCu wire, the creation of Cu_3Al_2 IMC was inhibited. Pd layer can act as a barrier for Cl^- penetration and also reduces the formation of CuAl IMC. More recently, Gan et al. [184] conducted HAST tests on PdCu wires and compared the reliability with that of Au wires. Their results are summarized in Table 6.2. PdCu wires have higher characteristic life than Au wire.

6.1.3 Failure Model and Acceleration Factor for Humidity Tests

Bond pad corrosion failures are accelerated by uHAST and bHAST tests. The accelerated corrosion test results are extrapolated to field-use conditions using physics of failure models. The models use the product of an RH term, an applied

Table 6.2 HAST data comparison for Au and PdCu packages [184]

Wire	Test	Test conditions	t_{first} (h)	t_{50}	$t_{63.2}$ (η)	β
PdCu	bHAST (3.6 V bias)	130 °C 85 % RH	1,817	3,593	3,849	5.06
Au	bHAST (3.6 V bias)	130 °C 85 % RH	1,553	2,584	2,752	4.96
PdCu	uHAST (unbiased)	130 °C 85 % RH	3,000	8,971	10,124	3.44
Au	uHAST (unbiased)	130 °C 85 % RH	4,000	9,222	10,189	2.82

voltage term, and a temperature-based Arrhenius factor. Two of the common models for humidity tests are discussed below:

Reciprocal exponential model [196]: $t_{\text{life}} = C_0 e^{\frac{b}{RH}} f(V) e^{-\frac{E_a}{kT}}$ where C_0 is an arbitrary scale factor, b is an empirical constant (~ 300 for AuAl), E_a is the activation energy (0.3 eV for AuAl), and $f(V)$ is an unknown function of applied voltage.

Power Law (Peck's model) [197]: $t_{\text{life}} = A_0 RH^{-n} f(V) e^{-\frac{E_a}{kT}}$ where A_0 is an arbitrary scale factor, n is an empirical constant, RH is the relative humidity, E_a is the activation energy, and $f(V)$ is an unknown function of applied voltage.

The mechanism of Au–Al corrosion has been primarily described by Peck's law. In an empirical study of THB/HAST (85/85, 100/85, and 5–70 VDC), E_a is the activation energy (76.22 kJ/mol), n is an empirical constant (2.66), and $f(V)$ is the voltage function (power law, ~ 1.5). Acceleration factors can be obtained by varying temperature, RH, or voltage for the test. The literature on Cu wire bond testing has not developed any acceleration factors yet. We have presented past studies on Au–Al bonds to provide guidelines for developing an AF and activation energy for humidity tests on Cu–Al bonds. In general, the temperature in the HAST testing is varied and RH is kept the same.

The modified model is given by $t_{\text{life}} = K_0 e^{-\frac{E_a}{kT}}$. A study by NASA reported a study on AuAl wire bond failures at 130 and 150 °C in air and in a humidity chamber at 85 % RH [198]. The mean life to failure was plotted against temperature in Arrhenius coordinates, and the activation energy was obtained, as shown in Fig. 6.9. The activation energy of wire bond failures under HAST conditions was 40.52 kJ/mol, whereas for dry air the activation energy was 146.66 kJ/mol. Acceleration factor values of 4.6, 22, and 1,500 were obtained for temperatures of 150 °C, 130 °C, and 85 °C, respectively.

Teverovsky et al. [198] reported the activation energy for bias HAST test conditions of 110 °C/85 % RH for 800 h, 130 °C/85 % RH for 360 h, and 150 °C/85 % RH for 130 h. The failure distribution was plotted for the above three temperatures (Fig. 6.10) and the activation energy was found (Fig. 6.11). The activation energy was obtained to be 56.93 kJ/mol.

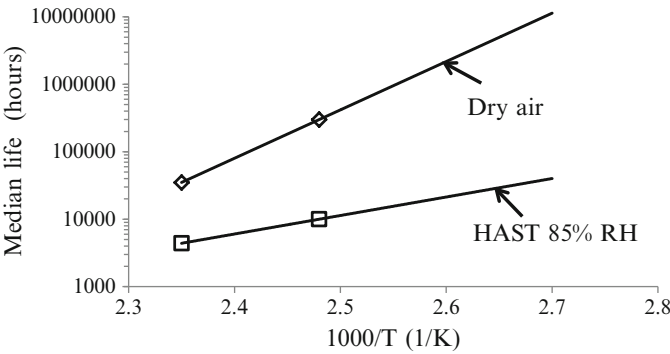


Fig. 6.9 Activation energy of corrosion in dry air and HAST conditions [198]

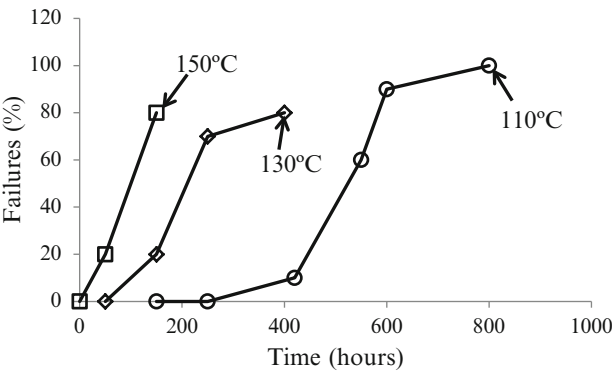


Fig. 6.10 Failure distribution of wire-bonded parts under HAST temperatures of 110, 130, and 150 °C/85 % RH [198]

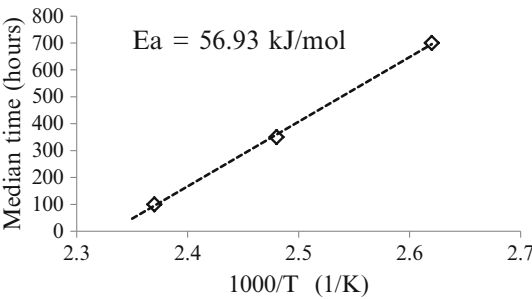


Fig. 6.11 Activation energy of wire bond failures under HAST [198]

The studies on humidity reliability tests on Cu wire-bonded parts are very limited, and as of now the activation energy of Cu wire-bonded part failures under humidity has not been reported. However, the method discussed in this section can help to obtain the activation energy for CuAl system.

6.2 Electromigration Tests

Electromigration is the transport of atoms in a conductor when stressed at high current densities. As of 2013, the literature on electromigration in Cu and PdCu wires on NiPdAu and NiPd finishes was sparse. However, the knowledge base obtained from experiments conducted on Au wires on Al pads can be used to conduct similar studies on Cu and PdCu wires on NiPdAu and NiPd finishes.

Failure mechanisms related to electromigration have been reported for Al in semiconductor devices [199]. The primary failure modes are voids at the cathode and hillocks at the anode under high current densities in the range of 10^6 – 10^7 A/m². High current densities also increase the growth of IMCs due to localized joule heating. For an Au–Al system, stable IMC systems have been characterized as AuAl₂, AuAl, Au₂Al, Au₈Al₃, and Au₄Al. Au₈Al₃ is the first to form by consuming the Al [200]. Au₄Al then grows, consuming the Au₈Al₃ and converting it to the Au₄Al phase. Voiding appears during the formation of the Au₄Al phase. Since the resistivity of IMCs is higher than the resistivity of Au and Al, the wire bond resistance increases as the IMCs grow. Figure 6.12 shows the resistivity values of the IMC phases observed in Au–Al and Cu–Al systems. The IMCs were found to have a resistivity an order of magnitude higher than pure metals [200]. Additionally, the resistivity of Cu–Al IMCs is lower than the resistivity of Au–Al IMCs, which can increase the reliability under electrical current loads.

6.2.1 Au–Al System

Orchard et al. [201] studied the influence of current densities on IMC formation for an Au–Al system with an Au wire diameter of 25 μ m. Ball bonds were 110 μ m in diameter and were arranged on a single bond pad to permit the four-point measurement of electrical resistance at a single junction (Fig. 6.13).

Electromigration tests were carried out at +5, +300, –300, +500, and –500 mA, and current densities were on the order of 10^6 A/m² [201]. As seen in Fig. 6.14, a positive current indicates that the direction of current was from Au to Al, while a negative current indicates that the direction of current was from Al to Au.

For 5 mA, current densities ranged between 1.5 and 15×10^6 A/m²; for 300 mA, current densities ranged between 90 and 900×10^6 A/m²; and for a 500 mA current, densities ranged between 150 and $1,500 \times 10^6$ A/m². It was found that the growth of IMCs is dependent on the direction of current, and the IMC thickness

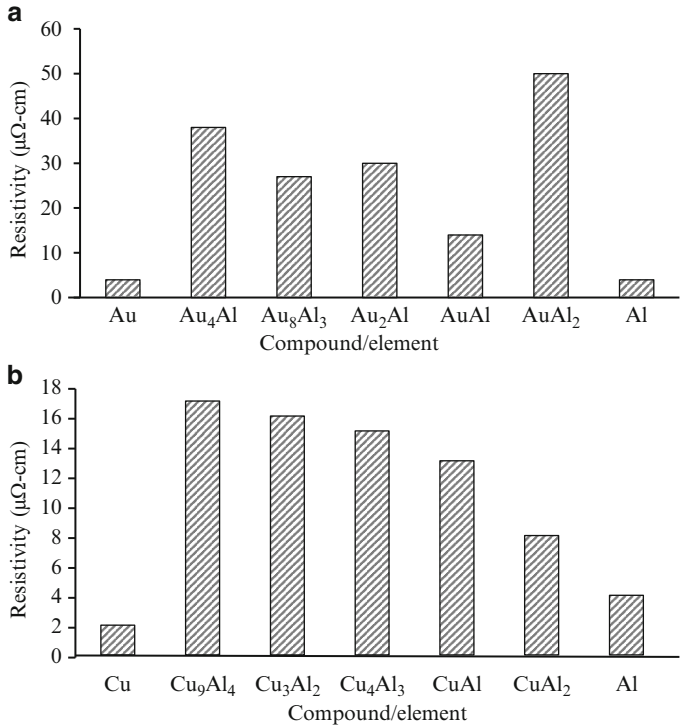


Fig. 6.12 Intermetallic resistivity for (a) Au–Al and (b) Cu–Al systems [200]

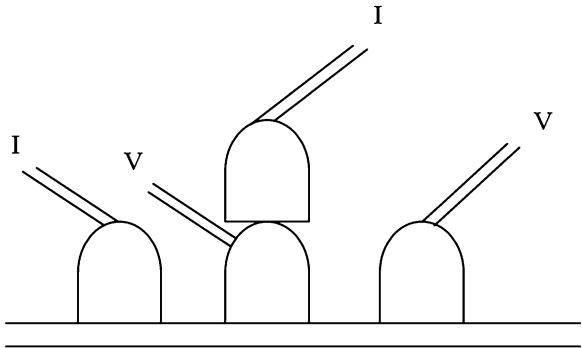
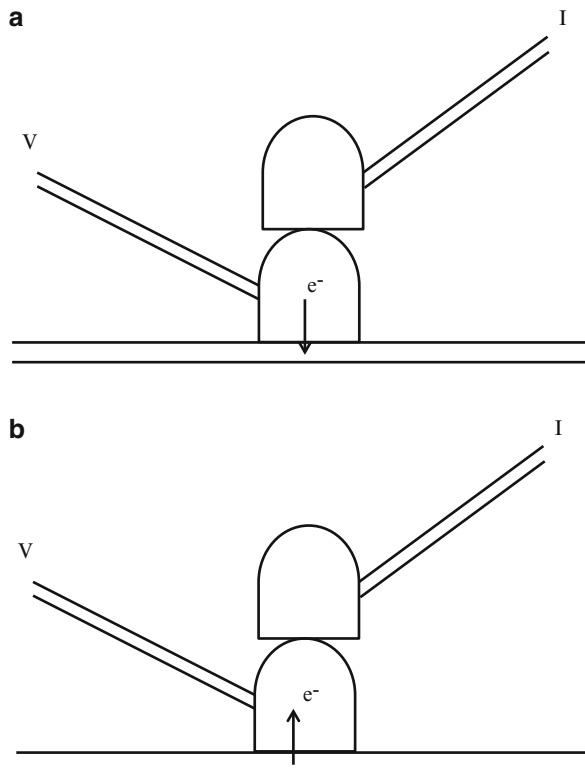


Fig. 6.13 Configuration showing wire bond layout (current (I) and voltage (V)) for four-point electrical resistance measurement between the Au wire and Al pad [201]

is proportional to the current density. Figure 6.15 shows the change in resistance versus current level. Positive (Au to Al) currents increased the rate of resistance change, whereas negative (Al to Au) currents increased the resistance less than positive currents [201].

Fig. 6.14 (a) Positive current (Au to Al) and (b) negative current (Al to Au) [201]



A microstructural evaluation showed the presence of Au_8Al_3 , Au_4Al , and Au_2Al IMC phases after just 3 h of aging at 170 °C under current levels of ± 500 mA [201]. It was also found that as the test progressed up to 24 h, the IMCs and voids grew in size. Figure 6.16 shows voiding at the interface of the samples aged for 24 h at 170 °C, where the direction of current was reversed after 16 h. Higher voiding was observed in the samples where the current was reversed, compared to samples under an entirely positive or an entirely negative current. Although voiding was more pronounced in the specimens where the current direction was reversed than in the positive current samples, the resistance values were found to be lower than the resistance values of the positive current samples. Hence, the dominant factor in increasing the resistance was intermetallic formation and growth, not voiding.

The effect of current polarity was reported by Zin et al. [202], where the influence of electromigration on the kinetics of contact failure and the effects of directionality on Au–Al wire bonding were studied. Electromigration tests were carried out under a temperature range of 150–175 °C and a current density of 5×10^4 A/cm². Interfacial resistance measurements and characterization of the interfacial microstructure were carried out to investigate the influence of

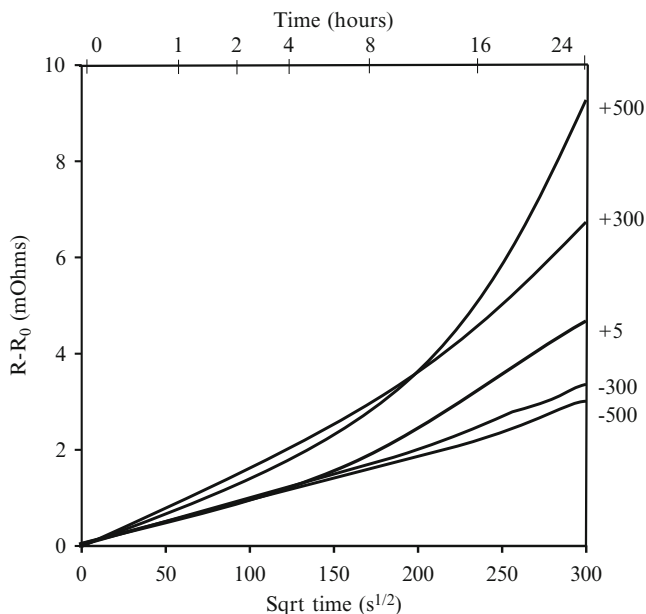


Fig. 6.15 Resistance change vs. $t^{0.5}$ for wire bonds at 170 °C, with imposed currents of +500, +300, +5, -300, -500 mA [201]

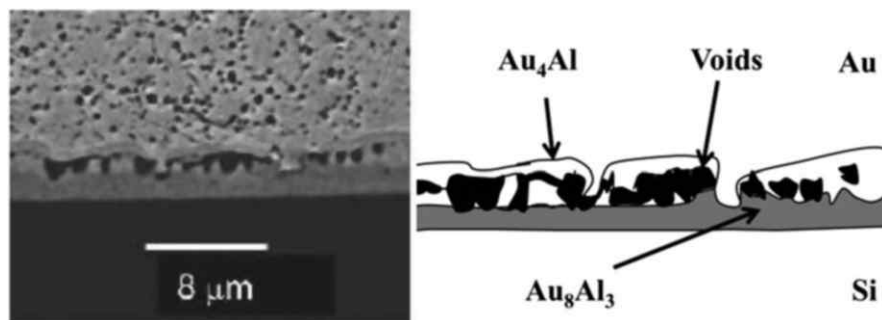


Fig. 6.16 Au–Al interface after aging at 170 °C for 24 h under current (+500 mA) that was initially positive but was reversed (–500 mA) after 16 h [201]

electromigration on the failure rate of Au wire bonds on an Al pad (1 μm thick). As shown in Fig. 6.17, the contact resistance between the Au wire and the Al pad showed that the failure rate was dependent on the direction of electron flow across the contact, where an electron flow from Au to Al (positive current) resulted in a faster failure rate than in the opposite direction (negative current).

Examinations of the microstructures of Au–Al contacts (a) without current, (b) with electron flow from Au to Al, and (c) with electron flow from Al to Au, were

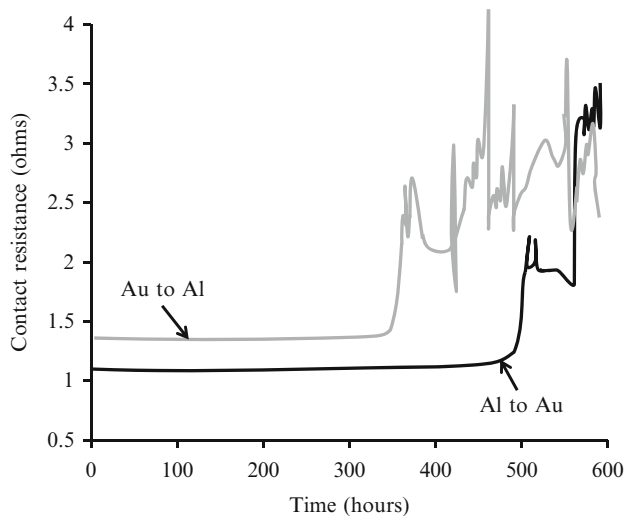


Fig. 6.17 Contact resistance vs. time on 99.99 % Au wire contact tested at 170 °C under current of 0.25 A [202]

conducted [202]. Voiding was observed between the Au wire and IMC layer. For both current directions, the Al pad turned into one primary IMC phase, an AuAl IMC, which formed and remained at the interface. The contacts in which the electron flowed from Au to Al formed an additional IMC (IMC2) between the initial IMC and Au ball, AuAl_2 , which contained a higher Al concentration than the underlying AuAl IMC. The IMC2 layer was mixed with voids and appeared grainy and porous under SEM.

Failure was delayed when the electromigration force was directed from the Al to the Au wire, because the rate of Al consumption was impeded by the electromigration force. Electromigration can accelerate or decelerate the growth rate of IMCs, affecting the failure kinetics. Failure was accelerated when the electromigration force was directed from Au to Al because it made the IMC phase grow faster.

Failure mechanisms related to electromigration were discussed for Au–Al systems in this section. Since the resistivity of Cu–Al IMCs is lower than that of Au–Al IMCs, a Cu–Al system has a different reliability under electrical current loads. As of 2013, the effects of electromigration on copper wire bonding had not been well examined. Studies to analyze the effects of high current on IMC formation are recommended for alternative wire bonding metallurgies, such as Cu wire or PdCu wire on NiAu and NiPdAu pads. Additionally, the effects of current reversal must be studied to understand the growth behavior of IMCs under the usage life of electronics.

Table 6.3 Activation energy for electromigration

	E_a (kJ/mol)	Current density (A/cm ²)	Temp (°C)	Reference
Al	60.79	$1\text{--}2 \times 10^6$	175–350	[203]
Au–Al IMC	73.323	10.19×10^2	400–500	[204]
Al (0.5 % Cu)	83.94	1.2×10^6	260	[205]
Al–4 % Cu/TiW	55.00	1.5×10^7	275	[206]
Al–2 % Si	40.52	1.5×10^7	275	[206]
Cu	74.29	1.5×10^7	275	[206]
Cu	62.72–98.42	6.0×10^6	200–250	[207]

6.2.2 Failure Model and Acceleration Factor for Electromigration Tests

The time to failure under electromigration is modeled by Black's equation [199]:

$$t_f = A_0 \times J^{-N} e^{\left(\frac{E_a}{kT}\right)}$$

where t_f is the time to failure, A_0 is a constant, J is the current density, N is a constant, E_a is the activation energy for the electromigration failure, k is the Boltzmann constant, and T is the temperature in Kelvin. Table 6.3 lists the activation energy for electromigration in Al, Cu metals, and Au–Al IMC systems.

The acceleration factors under electromigration tests can be obtained by varying either the current density or the temperature and then obtaining the ratio of times to failure.

6.3 Summary

High humidity, high temperature, and high current densities can affect the reliability of Cu wire bonds. The combined effects of temperature and humidity on wire bond strength can be estimated using a PCT and a HAST. In high-temperature and high-humidity environments, copper oxidation at the interface of the Cu–Al bonding region causes cracks and weakens the Cu–Al bond. The literature suggests that pH and Cl levels in the mold compounds should be minimized to maximize HAST reliability. Researchers have evaluated the high humidity reliability of Pd-coated copper wire and have found that PdCu wires are more reliable than bare Cu wires. The bond–pad interface in bare Cu wire shows continuous cracking, possibly due to chlorine-induced corrosion, whereas there is no cracking in PdCu wire.

As of 2013, the literature on the effects of electromigration on Cu wire bonds is very sparse. The information obtained from the experiments conducted on Au wires on Al pads can be used to conduct similar studies on Cu and PdCu wires on NiPdAu

and NiPd finishes. Electromigration-related failures have been reported for Au–Al systems. The resistivity of Cu–Al IMCs is lower than that of the Au–Al IMCs, which can result in higher reliability under electrical current loads than in Au–Al systems. For Au–Al systems, positive (Au to Al) currents increase the rate of resistance change, whereas negative (Al to Au) currents have less influence on resistance change. Failure under electromigration is accelerated when the electromigration force is directed from Au to Al because the current makes the IMC phase grow faster than in an Al-to-Au system. Intermetallic formation and growth increase the resistance more than voiding does.

This chapter discusses the bond pads used in Cu wire bonding. The common bond pad materials used in the industry are introduced and explained. The high stiffness of Cu requires robust bond pads to withstand the stresses from the bonding process. In addition to normal compressive force, there are shear forces, which are applied due to the ultrasonic scrubbing action during bonding. These forces could damage the underlying pad metallization and easily fracture the stress-sensitive dielectrics. As discussed in the previous chapters, the high bonding force required for Cu wire bonding leads to Al splash. In order to minimize Al splash, nickel-based pads can be used. Nickel pads provide protection to the underlying pad metallization while providing enhanced package reliability. However, nickel is prone to oxide formation. Therefore, a noble metal layer of gold or palladium is deposited to provide robustness, resulting in several combinations of surface finishes, including NiAu, NiPdAu, and NiPd. The chapter also discusses different pad finish thicknesses and their effect on the reliability of wire bonds.

The bondability of pads is reduced by the pad surface contamination and surface oxidation. The chapter also discusses the sources of pad and lead surface contamination. Pad surface treatments, including oxide coating and plasma treatment to minimize pad contamination and remove surface oxides, are discussed.

7.1 Bond Pad Materials

Bond pad materials for Cu wire bonding require thicker and higher yield strength bond materials than in Au wire bonding. This section discusses the common bond pad configurations used in the industry.

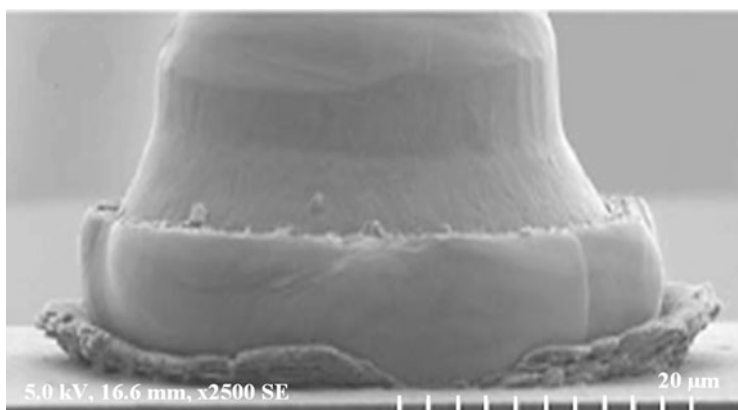


Fig. 7.1 Al splash: Cu bond on Al pad [78]

7.1.1 Al

The wire bonding industry has been using Al bond pads because they are inexpensive and easily wire bondable. It has been reported that a Cu–Al bond is more reliable and has a longer life than an Au–Al bond [156]. Additionally, Cu–Al intermetallics grow at a slower rate than Au–Al intermetallics and have a lower tendency to form Kirkendall voids at the ball bond–pad interface [93, 123, 152, 154]. However, the high stiffness of copper introduces difficulties during bonding to Al or Au surfaces. Pure Cu is about twice as hard as pure Au and is more susceptible to work hardening [208]. A higher bonding force (20–25 % higher than for Au) is required because of the higher hardness and greater work hardening [21, 54]. The deformation associated with wire bonding can increase the hardness of Cu by half. Thus, Cu wire bonding can result in up to 30 % higher pad stress than Au wire bonding [27]. This can cause pad peeling and dielectric cracking [209], and soft Al can also smear off during bonding along the ultrasonic direction, causing Al splash (Fig. 7.1) [78].

High-performance devices are increasingly relying on low- k (dielectric constant (k) < 3 [210]) materials under the bond pads to improve the capacitance, device speed, and signal integrity in Cu interconnects [211]. Since low- k materials are very soft and have low mechanical stiffness, Cu wire bonding can damage the circuitry under pad (CUP). Ultralow- k materials are being used in the semiconductor industry; these materials are produced by incorporating porosity into the existing low- k materials, which increases the risk of pad damage. While the higher bonding force risks pad and CUP damage, the lower force will lead to nonstick-on-pad (NSOP). Bond over active (BOA) technology is another development for miniaturization of semiconductor devices. It enables the use of a “keep-out zone” underneath the bond pad by moving the devices, ESD circuitry, and power and ground buses underneath the bond pads. The implementation of fine-pitch, low- k , and BOA technology in

wire bonding has led to several new metal-lift failure modes such as aluminum cap lift, copper metal lift, and tilted metal lift, which are observed under the ball shear and wire pull tests [212].

Ultrasonic energy is employed in Cu wire bonding to break the surface oxidation of the free air ball (FAB) to improve the interfacial adhesion between the FAB and bond pad, as well as to soften the FAB and increase the bonding interface temperature [60]. As a result of the application of ultrasonic energy during bonding, shear forces add to the already applied normal bonding force. Such shear stress can transmit through the bond pad metallization to the brittle, easily fractured dielectrics underneath, leading to pad peeling and bond failure. Since the ultrasonic energy is applied in the horizontal direction without a vertical bonding force in the area, the contact at peripheral areas is weak. The ultrasonic energy can cause an initial crack in the ball periphery, which can then propagate under high-temperature storage as well as under corrosive environments, decreasing the bond reliability [213].

Al splash or Al bond pad squeeze is observed in Cu wire bonding because of the lower flow stress of Al as compared to Cu [60]. Although Cu wire bonds can achieve higher shear strength values than Au ($182.47 \mu\text{N}/\mu\text{m}^2$ vs. $121.64 \mu\text{N}/\mu\text{m}^2$), the amount of Al splash increases linearly with the shear per unit area [59]. Therefore, the shear strength must be limited by the minimum Al thickness under the bond pad (remnant Al). The remnant Al under the Cu bonds is less than that in Au bonds because of the higher Al splash [214]. The remnant Al is required to maintain bond reliability, since remnant Al that is too thin can be completely consumed by the Cu–Al IMC, leading to bond failure [127, 215]. Al splash can damage the fragile dielectrics under the pad and can also result in electrical shorting of the bond pad with adjacent pads when the splash is larger than the pad pitch.

Pad cratering can be prevented by selecting the appropriate bond pad metallization, thickness, and structure, and optimizing the bonding parameters [216]. Researchers have adopted several approaches to reduce pad damage, such as increasing the bond pad hardness by doping the bond pads with Si or Cu [123], using softer Cu wire along with optimized bond force and ultrasonic power [27, 30, 73, 209], using harder metallization finishes [23, 57, 115, 217], and using more robust underpad structures.

One way to reduce the ultrasonic bond stresses is to select a softer Cu wire or reduce the ultrasound level [209]. Shah et al. [27] demonstrated that adopting a softer Cu wire resulted in a 5 % reduction in ultrasonic force. Also, a reduction in the ultrasound level caused the ultrasonic force to be reduced by 9 %. It has been reported that by using softer wire along with optimized force and ultrasonic power, 39 % lower pad stress than Au wire can be achieved [73]. Shah et al. [218] also reported that by using a 7–9 % lower ultrasound level, the pad stress can be reduced by 42 %. England et al. [28] optimized the bonding force, and the ultrasonic parameters were optimized at bonding temperatures of 150 and 175 °C. It was found that these increased temperatures resulted in a reduction of the bonding force, which in turn can minimize the occurrence of pad cratering.

Another solution to pad cratering is to modify the chip design for Cu wire bonding by using a robust underpad structure and an optimal Al pad thickness [219, 220].

As mentioned earlier, Cu wire bonding on Cu/low- k structures is challenging because the low- k polymers are encased in brittle diffusion barriers which can crack during bonding. Special underpad support structures need to be designed [221]. Chen et al. [220] recommended using an Al layer thicker than 0.8 μm to prevent damage to the pad structure. For Al thicknesses below 0.8 μm , the underpad structure and via distribution need to be optimized to prevent damage to the pad structure. England et al. [219] conducted a study on the influence of barrier layer structure and composition on the presence of pad cratering, and the use of titanium nitride (TiN) as the barrier layer resulted in a high occurrence of cratering. Pad cratering was absent in Ti and titanium tungsten (TiW) barrier metals, as well as in the configuration of TiN on top of Ti. Periasamy et al. [222] developed hybrid structures using the bottom 2–4 Cu–low- k stacks and the top 2 Cu/SiO₂ stacks. This structure addresses the problems of bond pad peeling, bond pad sinking, low ball shear, and damage to the underlying circuitry.

The performance and reliability of the Cu wire bonding process can be improved by understanding the microstructural and mechanical properties of FABs and the Cu–Al interface. Researchers have developed several methods, such as nanoindentation and atomic force microscopy, to measure and characterize the hardness of the FAB and the bonding wire [151]. Fan et al. [151] characterized the tensile properties of Cu wire before and after the EFO process by conducting pull tests. The hardening constant in the Hall–Petch equation, which determines the localized stress in the pad, was obtained. The measured material properties provided the inputs for the FEA model to characterize the dynamic response of Cu wire bonding on the Al pad [135, 211, 223].

Pads that are too thin or too thick are undesirable. A pad that is too thin cannot protect the CUP, whereas a thicker pad can have more Al splash and a higher risk of passivation cracks and pad shorts. Damage occurring during wafer probing should be examined, since probing might crack the dielectric layer under the pad. A few un-bonded devices should always be etched to see if cracks are present. The industry is exploring options to protect the underlying structures, such as harder pad metallizations. These options are discussed in detail in Sect. 7.2.

Al splash can be reduced using several methods. First, high-purity Cu wires can be used. Srikanth et al. [44] reported that higher purity wires have lower flow stress than lower purity wires due to having fewer grains. Because of the lower flow stress, a lower bonding force is required, which results in a lower Al splash. Second, a modified capillary design can reduce Al splash by allowing a lower ultrasonic power than the original design [216]. Third, the ball size can be reduced relative to Au to allow for splash. For many processes, shear and area show a direct correlation. To allow for splash, the ball size must be reduced, which in turn reduces the size of the Cu wire required [104, 215]. In general, Cu wires are made 2.54 μm thinner than Au wires. A special process, such as ProCu developed by K&S [54], is required for Cu to reduce the splash while still maintaining the shear per unit area. Finally, the Cu wire ball and pad can be made to rub against each other in a direction intersecting the ultrasonic wave application direction, minimizing Al splash [224].

Table 7.1 Bonding conditions for different wire–cap combinations [154]

Bonding parameters	Au wire–Al cap	Au wire–Ni/Au cap	Au wire–Ni/Pd/Au cap	Cu wire–Al cap	Cu wire–Ni/Au cap	Cu wire–Ni/Pd/Au cap
Force (N)	0.69	0.69	0.69	0.25	0.25	0.25
Ultrasonic power (mW)	70	60	60	80	100	60
Time (ms)	30	40	40	40	40	40
Die temperature (°C)	150	150	150	150	150	150

7.1.2 Cu

Cu metallization has replaced Al as the preferred interconnect because it has better electrical performance and higher speed for fine-pitch applications. However, Cu is harder than Al and prone to oxidation; therefore, it cannot be easily probed and wire bonded. Coating Cu pads with a noble metal, such as Au and Pd, or a harder metal, such as Ni, addresses these problems [225]. However, Ni is not bondable by itself, as it forms an oxide layer upon exposure to air. To provide a bondable surface, Pd or Au plating is applied on top of Ni. Electroless Pd is a cost-effective alternative that provides a bondable surface for Cu wire bonding. The NiPdAu surface finish has a diffusion barrier provided by Pd and Ni. NiPdAu is applied on Al pads, but it can be applied over Cu as well.

The mechanical reliability of wire bonding depends on the intermetallic compounds formed at the bond–pad interface. The bonding of Au or Cu on a Cu pad is challenging because of the tendency of the copper metallization to oxidize. For this reason, bare copper pads are not used in the industry. Capping the Cu bond pad surface is one of the approaches for providing a reliable, probe-able, and wire-bondable surface [225]. Table 7.1 presents bonding process variations for several metallurgical combinations. It can be seen that a lower force value is required for Cu wire bonding compared to Au wire. Cu wire bonding takes a longer time and higher ultrasonic power to bond than Au wire [154].

7.2 Over Pad Metallization/Pad Finishes

Bare Al pads are soft, resulting in Al splash due to the high force required during Cu wire bonding [60, 78]. Nickel (Ni) provides a surface hardness that can withstand the load from copper wire bonding. Ni is about 50 % harder than Cu and four times harder than aluminum, so it provides greater protection against the higher stress resulting from Cu ball bonding, as well as damage during probing. This is especially beneficial for devices with low-*k* active circuitry under the bond pad [23, 57, 115, 217]. Ni-based pads also increase the bonding parameter window, especially when higher ultrasonic energy is used. Ni-based finishes have the advantages of high reliability, high bonding load, protection of fragile structures, compatibility between probing and bonding, and compatibility with Au and Cu wire bonding.

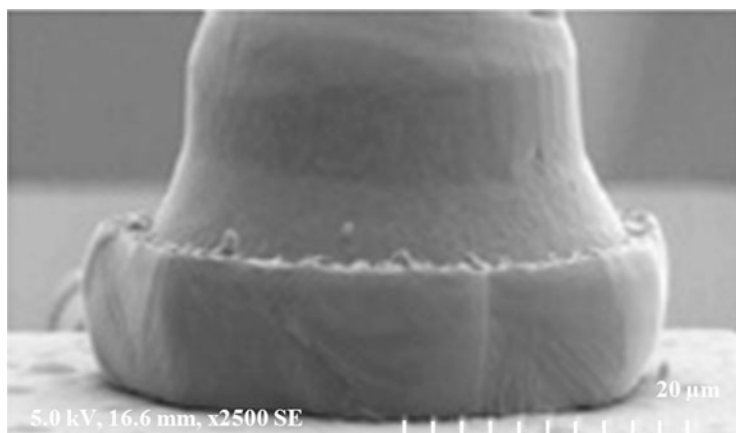


Fig. 7.2 A Cu bond on a NiPdAu pad (no Al splash) [217]

Typically, a layer of Ni 1–3 μm thick is deposited on either the Al or the Cu base metallization as the surface finish. A Ni layer by itself is not easily wire bondable because it forms a layer of surface oxide, which is hard and unbreakable. Therefore, a thin noble layer of Au and/or Pd is required on top of the Ni for more robust manufacturability, bondability, and reliability. Typical thicknesses are 0.03–0.05 μm Au, 0.1–0.3 μm Pd, and 1–3 μm Ni [58].

Au provides an excellent bondable surface, but it is an expensive metal. Therefore, owing to cost considerations, the electronics industry is considering several options, such as a palladium layer between the nickel and gold or pure palladium. The use of palladium thins down the Au layer and improves the corrosion resistance of the nickel layer. The diffusion of Ni, Cu, or Au into Pd is slow; therefore, it provides highly reliable bond–pad interfaces. Palladium-based surface finishes are Au or Cu wire bondable with wide bonding process windows, high pull strengths, and tight standard deviations. Although Pd prevents the diffusion of Ni into the bond, thick Pd is undesirable since Pd segregation at the interface presents a reliability concern. In Ni finishes, an optimal Pd thickness needs to be determined to limit the Ni diffusion to the surface and its effect on bonding, especially if humidity is a factor. Pd and Au interdiffusion does not affect bondability, but could cause the failure mode to change locations from the neck to the heel of the joint. Ni-based pads such as NiAu, NiPdAu, and NiPd have good reliability and no Al splash (Fig. 7.2). NiPdAu pad metallization can be applied on both the existing pads and the Cu conductors in semiconductor dies.

Anh et al. [57] compared the shear and pull strengths of Cu wire bonded onto Al and NiPdAu pads. They reported that for as-bonded specimens, NiPdAu pads showed a 30 % higher shear strength per unit area than the Al pads. High-temperature aging was carried out at 225 °C for up to 2,000 h, and it was found that the ball shear strength for NiPdAu pads remained stable, as compared to Al pads. The failure mode for NiPdAu pads for as-bonded specimens was through

the ball, leaving a thin layer of Cu on the pad, which did not change with aging. Shearing through the ball indicates a strong interfacial strength. The wire pull strength on NiPdAu pads and the failure mode, wire-mid-span breaking, did not change with aging. For Al pads, the wire pull strength dropped after aging at 225 °C for 96 h due to a change in the failure mode from wire-mid-span breaking to pad peeling. The package-level reliability stresses after 1,000 air-to-air temperature cycles (−65 to 150 °C), 240 h of uHAST, and 1,620 h of high-temperature baking at 175 °C on pad configurations showed that both bare Al and NiPdAu–Al pads had equal reliability. Bare Cu wire bonding on NiAu laminate pad finish has also been used in the industry due to its good reliability performance. Due to the prohibitive cost of Au, ENEPIG finish is also gaining momentum as an alternate finish for bare copper bonding.

A study conducted by Chylak et al. [217] reported no significant differences in the shear strengths for NiAu, NiPdAu, PdAu, electroless nickel immersion gold (ENIG), electroless nickel/electroless palladium/immersion gold (ENEPIG), and electroplated silver. Studies have been conducted to investigate Ni-based finishes for wire bonding [226–228]. It was observed that for Cu, electrolytic Ni/soft Au performed well compared to Pd-based plating. Electroless Ni/electroless Pd (ENEP) was found to perform well in bondability, but ENEP with 4–6 % Pd offers a narrow process window compared to ENEP with pure Pd. Pure copper wire was found to attach well with the Pd layer, whereas PdCu wire attaches to thick Au layers [226]. Bonding data for Ni/thin palladium/Au finishes showed that as-received samples bonded well, whereas samples subjected to 85 % RH/85 °C for 12 h before bonding did not bond. Excessive first bond misses were encountered while bonding samples after humidity storage. High-temperature and reflow preconditioning did not degrade pull strengths, but increased the number of heel failures [228]. Johal et al. [227] compared electrolytic Ni/electrolytic Au (ENEA) with ENEPIG, and found pull strengths of about 0.078 N for a 30 µm wire for both finishes. However, bond shear tests indicated a higher average shear force for ENEPIG than for ENEA. Heel failures increased after preconditioning, while first bond misses were observed after humidity storage, along with an increase in standard deviation for both failure modes.

Johnson et al. [228] examined Au wire on thin Pd/Au plating on laminates and reported pull strengths in the range of 0.069–0.078 N for as-bonded structures and bonds that were preconditioned at 125 °C for 12 h. Those bond strengths are higher than the 0.029 N minimum pull strength established in MIL-STD-883. No first bond misses were observed. In the study, the primary second bond failure mode was found to be neck break above the ball, indicating a robust joint. Johnson et al. [228] also examined the effect of high-temperature storage at 175 °C for a period of 16 h on bond strength and found that when there is no Pd, a Au thickness of >0.3 µm is required to obtain good wire bond values in bond strength tests. A higher Au thickness in the range of 0.3 µm showed a strength of 0.113 N, whereas a thickness in the range of 0.05 µm showed a strength of 0.064 N. Compared to 0.3 µm Au thickness with no exposed underlying metal, a thinner Au thickness resulted in exposed metal. Since Au is a soft and ductile metal, it requires an optimal level of thickness to prevent degradation of the underlying metal.

However, the application of Ni-based finishes is difficult, and the industry is struggling to develop plating processes for these finishes. Capillary lifetime is another issue with Cu wire bonding, especially for Ni-based finishes. Ni and Pd are hard, so it is difficult to bond onto them. The yield decreases from one to two million bonds per capillary on Al pads to 100–200k bonds per capillary for Ni-based pads. Cu wire can also be bonded on NiPdAu-Ag-plated and roughened NiPdAu-Ag-plated lead surfaces, although Li et al. [229] reported that packages with NiPdAu-Ag-plated lead frames showed delamination at the top of the die paddle after stress testing, while packages with roughened NiPdAu-Ag-plated lead frames showed positive results after stress testing. Other finishes such as ImAg have also been evaluated [230], but have been shown to be susceptible to corrosion-related failures and, thus, are not gaining popularity.

The finish for laminate pads should be determined based on operating environments, reliability, and cost analysis.

7.3 Pad Finish/Metallization Thickness

Researchers have investigated the effect of pad finish thickness on bond shear strength [217, 228, 231]. Several thickness combinations of NiPdAu finish were analyzed by varying the Ni thickness between 0 and 3 μm , Pd thickness between 0 and 0.3 μm , and Au thickness between 0 and 0.03 μm . The average shear strength per unit area was in the range of 182.47–212.88 $\mu\text{N}/\mu\text{m}^2$ and was comparable for all finish combinations. However, the shear strength of Ni-based pads was double that of Al-based pads. Figure 7.3 shows several cells from A to H with different combinations of pad finish thickness for Ni, Pd, and Au. The Al pad was the reference for the experiment. No difference in shear strength/area was observed between the Ni-based pads, but the aluminum pad cell had a lower shear strength. Failure analysis revealed the failure to be located at the pad interface for the aluminum pad, whereas it was in the ball sphere for Ni-based pads, which is the

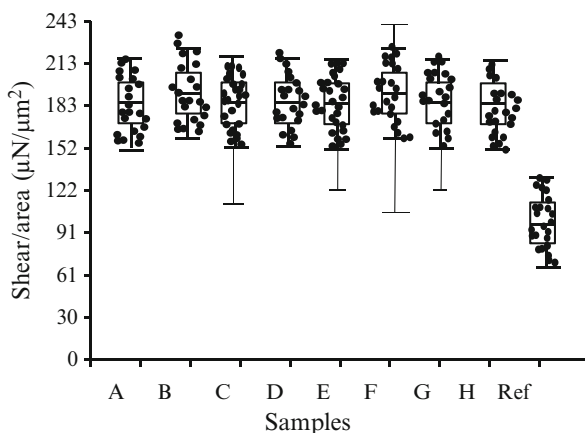


Fig. 7.3 Comparison of pad finish thickness combinations [217]

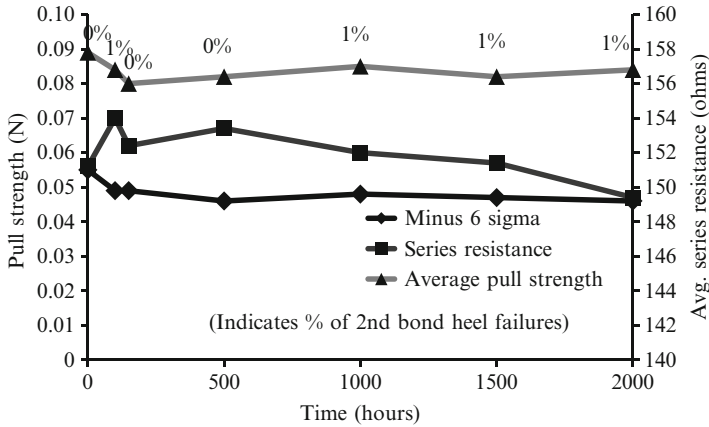


Fig. 7.4 High-temperature (125 °C) storage results for thin Pd/Au (0.3 μm/12.5 nm) finish [228]

desirable failure mode in shear testing. Failure at the pad interface indicates a weaker IMC for the aluminum bond pads than the Ni-based pads.

Johnson et al. [228] conducted high-temperature (125 °C) storage tests on several finish thickness combinations of Ni/Pd/Au for up to 2,000 h, and found no decrease in the pull strength or electrical resistance between the thicknesses, indicating that there was no detrimental intermetallic or void formation. Figure 7.4 shows the pull strength and average series resistance of thin Pd/Au (0.3 μm/12.5 nm) finish. There were no second bond lifts with any of the samples after aging, and the percentage of second bond heel failures did not change significantly with the high-temperature storage.

Leng et al. [231] investigated the effect of Ni thickness on the wire pull and ball shear strengths for as-received and 225 °C/15 h aged specimens. They reported that the Ni thickness of 1 μm could not support high bond forces and exhibited bond pad deformation, whereas 2 and 3 μm pads could sustain a high bond force and no pad deformation was observed. For cost savings, 2 μm thick Ni was recommended.

7.4 Factors Affecting Pad Bondability

Pad bondability is affected by the surface condition. Contamination from plating impurities and organic contamination on the pad surface degrade the pad bondability. The thickness of plating layers, surface contaminants, surface roughness, and hardness of the pad all affect the bondability and reliability of the bond pads.

7.4.1 Pad Contamination

Contamination on the pad surface may cause corrosion and reduce the bondability of the pad and, hence, the bond strength [232]. Contamination may also cause early failures during burn-in and in the field. The bond pad contaminants include both

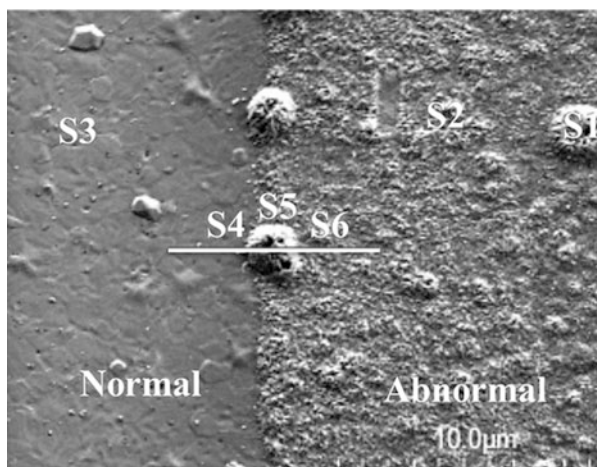


Fig. 7.5 SEM inspection of an abnormal pad [233]

organic and inorganic substances such as fluorine, chlorine, carbon, silicon metals, and metal oxides. These contaminants can originate from plating baths, outgassing of materials such as solder mask and adhesives, and the bonding environment, and may occur during the wafer fabrication process, transportation, storage, and assembly of the devices [232]. Yu et al. [233] reported bond pad abnormalities from contaminants as an issue in wafers, resulting in ball lift. Pads had a film containing Al, C, O, and Si on the native oxide. This contamination was suspected to have been caused by wafer processing. Figure 7.5 shows an SEM micrograph of the pad surface showing contamination. Inspection was done on locations S1 through S6 to assess the contamination. Locations S1, S2, S5, and S6 show abnormal pad regions whereas S3 and S4 show normal pad locations.

Another abnormal pad had a similar defect pattern. An EDX line scan (Fig. 7.6b) on the TEM sample (along line 1 from top to bottom in Fig. 7.6a) indicated the presence of Al, F, O, and K. It was concluded that potassium (K) from the packaging paper used for shipping the wafers caused the contamination. The common pad contaminants are discussed below.

7.4.1.1 Fluorine, Chlorine, and Carbon

Several processes can lead to fluorine, chlorine, and carbon contamination, including residual from the etchant used to remove final passivation dielectric layers and wafer packaging foam material. The fluorine-containing gases, such as freon, can be released as residual fluorine on metal pads as bonded or free AlF_3 . Fluorine contamination on the Al pads under 50 % relative humidity causes the formation of $\text{Al}(\text{OH})_3$ and Al/fluorine compound crystallites, which inhibits the growth of the self-passivating alumina layer, which is a barrier to oxidation [234]. Since IMCs form in areas where the alumina layer is fragmented during bonding, a thick

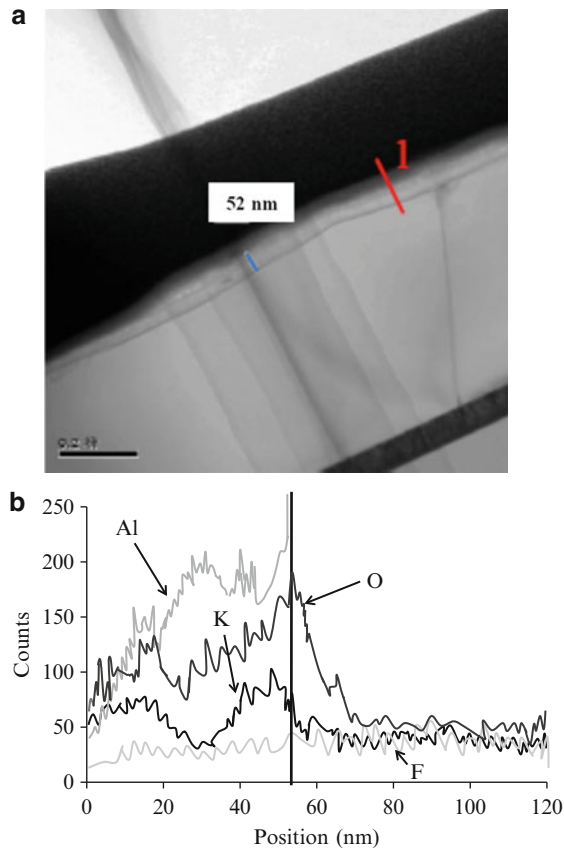


Fig. 7.6 (a) TEM inspection of an abnormal pad; (b) EDX analysis along line 1 (from the top down) [233]

alumina layer is not desirable. High fluorine contamination can result in a thick alumina layer on the bond pad, which leads to inadequate bonding [233, 235].

7.4.1.2 Oxygen

The source of oxygen on contaminated pads is the $C(O)$, $Al(O)$, and $Al_xF_yO_z$ formed during or after the pad opening process. Reactive epoxy diluents form an organic film and self-polymerize to reinforce the oxide layer on the aluminum bond pad [233].

Petzold et al. [236] investigated the influence of oxide film thickness on wire bonding behavior and the hardness of the Al pad surface using indentation testing, wire bond tests, and electron microscopy. Oxide film thickness values larger than 20 nm obstructed the bond contact and resulted in poor bonding quality. Figure 7.7 shows the influence of oxide film thickness on bond strength. It was observed that at over 20 nm, the occurrence of bond liftoffs and shear liftoffs increased. Therefore,

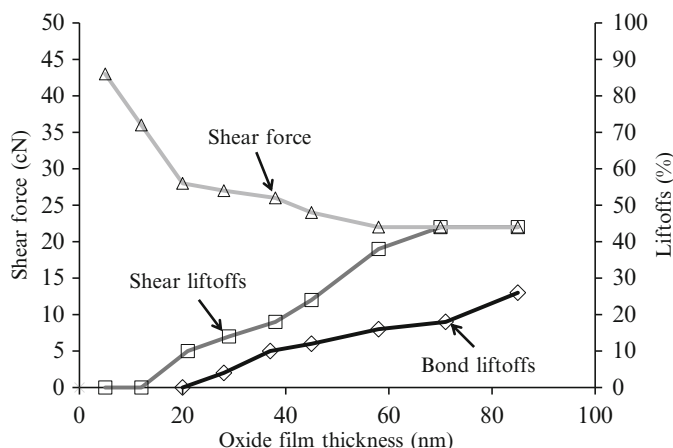


Fig. 7.7 Bond shear strength as a function of oxide film thickness [236]

wire bond quality decreased with 20–30 nm oxide films. The presence of such enhanced oxide films with thicknesses of more than 20 nm can be detected using indentation tests.

7.4.1.3 Silicon

Another element that can contaminate the bond pad is silicon. Contamination has been found after die sawing, where SEM observations have shown silicon contamination in the shape of a C-curve [233]. A C-curve is typical of residues left behind after the water rinse step in the dicing operation of the die.

7.4.1.4 Titanium

Titanium (Ti) contamination has been found on bond pad surfaces as a result of steps in the manufacturing process. This contamination is due to titanocene, which is used as a radical starter in a certain polyimide resin, where radical generation is carried out by electron transfer from titanocene chlorides to epoxides. Puchner et al. [237] investigated oxide formation and Ti distribution on aluminum bond pads. Ti layers of different thicknesses in the nanometer range (2, 6, and 10 nm) were deposited by means of physical vapor deposition, either directly after aluminum deposition or after an air break, in order to study their effect on wire bond quality. Depth profile measurements were carried out with time-of-flight secondary ion mass spectrometry (TOF-SIMS), which is a surface analytical technique that focuses a pulsed beam of primary ions onto a sample surface and produces secondary ions in a sputtering process. These secondary ions (both negative and positive) can provide information about the molecular composition of the upper atomic layer of solid surfaces. TOF-SIMS can detect contamination at low levels, high sensitivity, high quantification accuracy, and good depth resolution.

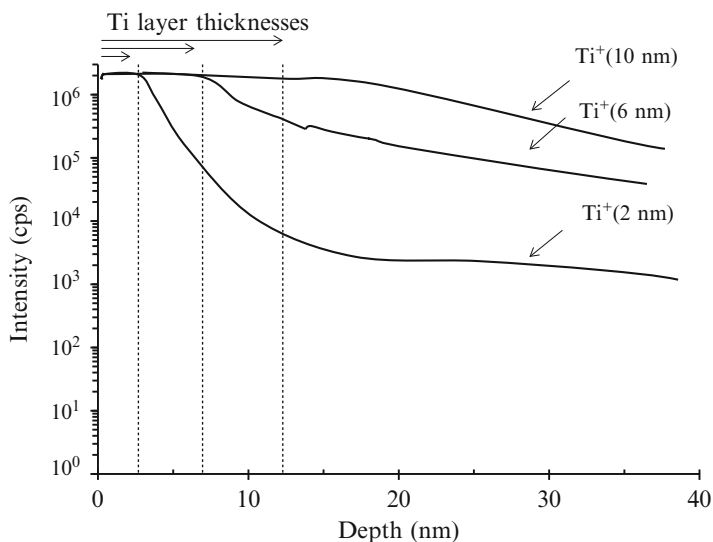


Fig. 7.8 Depth profile of samples with 2, 6, and 10 nm Ti thicknesses measured in the positive mode (500 eV O₂) [237]

Figure 7.8 shows the TOF-SIMS profiles of samples measured in the positive mode (positive ions). Native oxidation of the titanium slightly increased the thicknesses of the deposited layers. The effective thicknesses of the samples with Ti thicknesses of 2, 6, and 10 nm were about 3, 8, and 12 nm, respectively. Reduction of the sputter energy to 500 eV enabled a clear determination of the different thicknesses. Figure 7.9 shows the TOF-SIMS profile without any titanium deposition measured in the negative mode. It shows the self-passivating oxide formation of aluminum alloys after contact with oxygen. The oxide layer had an approximate thickness of 6 nm. Silicon and Cu did not contribute significantly to the surface oxide.

7.4.2 Lead Frame Contamination

Wedge bonding failures due to nonstick-on-lead (NSOL) have been reported for Ag-plated lead frames during second bond formation in thin quad flat packages [238]. The primary cause of failure after X-ray photoelectron spectroscopy and design of experiment verification was identified to be Cu ion contamination due to badly controlled pH levels during the plating process. Controlling the pH during the plating process removed the Cu contamination, which in turn eliminated the NSOL failures. The lead frame achieved an average wedge pull strength of 0.059 N after removal of the Cu contamination, as compared to 0.047 N before contamination removal (Table 7.2).

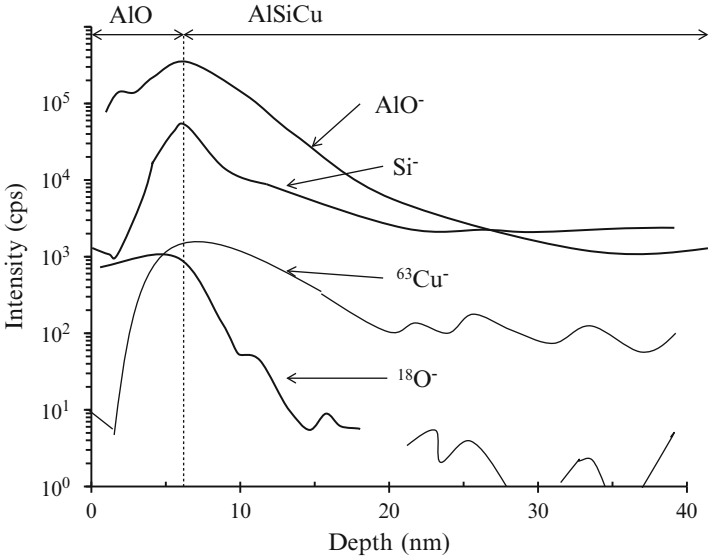


Fig. 7.9 TOF-SIMS depth profile of the AlSiCu metallization measured in the negative mode (Cs 500 ev) [237]

Table 7.2 Comparison of NSOL failures before and after contamination removal [239]

	NSOL failure (number of stoppages, out of 1,280)	Minimum wedge pull test (N)	Average wedge pull test (N)
Before	11	0.029	0.047
After	0	0.046	0.059

7.4.3 Pad Surface Roughness

The thickness of plating layers, surface contaminants, surface roughness, and hardness of the pad all affect the bondability and reliability of the PCB substrate [239, 240]. Rooney et al. [240] compared the color, reflectivity, and surface texture of PCB plating between bondable and non-bondable surfaces (Fig. 7.10), and they found that samples with thin gold plating were wire bondable, but performed poorly in high-temperature storage reliability tests. The wire-bondable gold had a shiny yellow color and a smooth appearance, while the non-bondable gold was brown and rough in appearance.

Smooth surfaces have better wire bonding than rough surfaces. However, pads with high surface roughness can still be wire bonded, although they are more prone to bad bonds than pads with smooth surfaces. Rough surfaces are problematic for bonding due to the reduced contact area between the bonding wire and the substrate pad. Also, rough surfaces are prone to contaminant entrapment, resulting in bond failures. Surface roughness can be decreased by grain-refining agents and

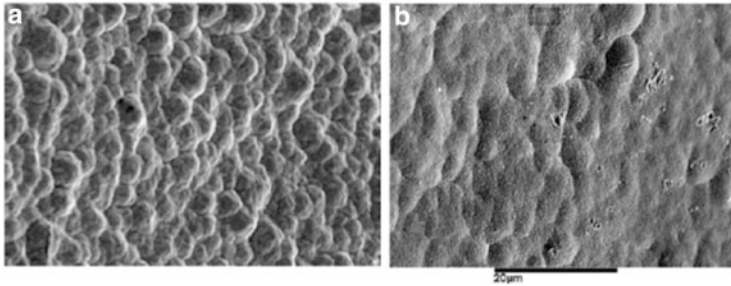


Fig. 7.10 SEM images of plating: (a) Rough appearance and poor wire bondability; (b) smooth appearance and good wire bondability [240]

increased by the increase in current density used in the Au and underlying Ni-plating processes.

Plating roughness is dependent on the finish. Li et al. [241] compared ENEPIG with NiAu. Observations by SEM reported that the granule size of ENEPIG finish was up to $9.0\text{ }\mu\text{m}$. ENEPIG has high surface roughness, expressed as Ra (arithmetic average of roughness) and Rq (root mean square of roughness). The Ra in traditional electrolytic NiAu finish is about $0.306\text{ }\mu\text{m}$, and the traditional Rq is $0.385\text{ }\mu\text{m}$. The roughness value of ENEPIG is more than twice that of NiAu finish. The differences in surface morphology between ENEPIG and electrolytic NiAu are caused by the different deposition methods used for these finishes. Since the Ni layer of ENEPIG finish is formed by a spontaneous crystal growth, the surface roughness of the Ni layer decreases with increasing Ni layer thickness. If the pretreatment (which is supposed to eliminate the roughness of Cu) before the plating of electroless Ni is not properly conducted, then the wire bonding performance decreases.

7.5 Bond Pad Surface Treatments

Bond pad surface treatments are used to clean the bond pad surface in order to enhance the bondability of the pad surface. The common treatment methods are organic coating on the pad and plasma treatment.

7.5.1 Organic Coatings on Pad

One method to clean the pad and minimize Cu oxidation is to coat the Cu bond pad with an organic coating [242, 243]. The application of organic coating is performed at the wafer level before dicing and provides protection up to the wire bonding process. Additional curing is carried out to minimize the oxidation of the organic-coated Cu pads. The application of a self-assembled monolayer (SAM) coating

enables the direct bonding of copper wires onto the copper bond pad without the use of plasma cleaning to remove the copper surface oxidation prior to wire bonding. Banda et al. [98, 243] evaluated the application of a SAM onto Cu wafers in a process that involves wet cleaning of the surface and immersion in a SAM solution. The SAM coating protected the Cu surface during the wafer dicing and die attach curing up to 150 °C. Lam et al. [242] reported that Cu wire-bonded parts assembled on organic-coated Cu pads passed a shear test up to 1,440 h of aging at 150 °C. Further characterization, qualification, and reliability tests need to be conducted on parts assembled with organic coating.

7.5.2 Plasma Treatment

Plasma treatment is a method of surface modification in which plasma-generated excited species react with a solid surface [244]. The plasma cleaning involves physical and/or chemical modification of the first few molecular layers of the surface, while the properties of the bulk material are retained. Plasma cleaning removes Cu oxides and organic contaminants from the bond pad surface [114, 141, 142] using gases—oxygen and argon or argon and hydrogen. Table 7.3 lists the common plasma gases used in wire bonding applications and the corresponding surface modification process.

Oxygen plasma is used for forming oxides, such as CO₂ and CO, with organic contaminants that can then be removed with a vacuum process, and argon plasma is used to etch away metal oxides and produce a clean, bondable surface. A mixture of argon and oxygen gas is utilized, followed by additional time in argon plasma only, as oxygen plasma is known to form oxides and is an aggressive plasma that can cause a parametric shift in semiconductor devices. The ratio of argon to oxygen is set to maximize the content of argon plasma and keep the oxygen plasma levels at a minimum. When argon is used in conjunction with hydrogen, physical cleaning is done by plasma, and hydrogen removes the oxides.

Plasma cleaning also increases the bond strength by acting as a surface modification technique. The effectiveness of plasma cleaning depends on the plasma parameters—power, plasma time, gases used in the plasma, and gas flow rate. The degree of plasma cleaning can be quantified using contact angle measurements. The shape of the liquid droplet depends on the surface tension between the drop and

Table 7.3 Plasma gases and surface modification process

Plasma gas	Surface modification process
Argon (Ar)	Contamination removal—ablation
Oxygen (O ₂)	Contamination removal—chemical
	Oxidation process (organic removal)
Hydrogen (H ₂)	Contamination removal—chemical
	Reduction process (metal oxide removal)

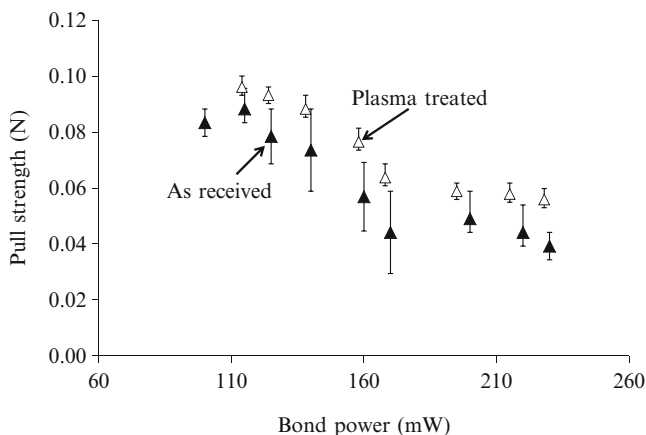


Fig. 7.11 Pull strength vs. bond power for 0.1 μm immersion Au-coated bond pads [245]

the bonding surface. In the case of a hydrophilic surface, the water droplet will spread out, forming a low contact angle, whereas in the case of a hydrophobic surface, the droplet will stand up on the surface, forming a high contact angle. Contact angle measurement tools are available that allow a controlled droplet amount and measurement of the contact angle between the droplet and surface.

Sivakumar et al. [114] reported the use of optimized plasma cleaning to remove the Cu oxide. Argon was used for physical plasma cleaning, and hydrogen was used to reduce the Cu oxide. An in-line plasma cleaning machine was used, which could be integrated with the wire bonding equipment to carry out cleaning prior to bonding. Different levels of argon and hydrogen were examined, and a DOE was conducted to optimize the exposure time, flow rate, and power. The effectiveness of oxide removal is assessed using auger electron spectroscopy to measure the remaining oxide thickness after plasma cleaning, where an oxide thickness of 50 Å is considered wire bondable.

The effects of plasma cleaning have been reported for electrolytic Ni, electroless Ni, electrolytic Au, and immersion Au [245]. In a study by Chan et al. [245], the electroless Ni thickness was 2.5–5 μm , the electrolytic Ni thickness was 4–8 μm , the electrolytic Au thickness was 0.11–0.7 μm , and the immersion Au thickness was 0.1 μm . They reported that the lowest bond powers for bonds decreased from 128 mW and 101 mW to 75 mW and 65 mW, respectively, after plasma treatment. The decrease in bond power was attributed to the reduction in ultrasonic energy (due to less pad contamination) during bonding. The pull strengths after plasma cleaning were all greater than 0.059 N, which was greater than the industrial lower threshold of 0.049 N. As seen in Fig. 7.11, the pull strength decreased with an increase in bond power.

In addition to pull strength, the extent of wire deformation was also characterized (Fig. 7.12). The extent of wire deformation provides information about the energy consumed in the bonding process. A large deformation corresponds to the high power required for bonding. Wire deformation is used as

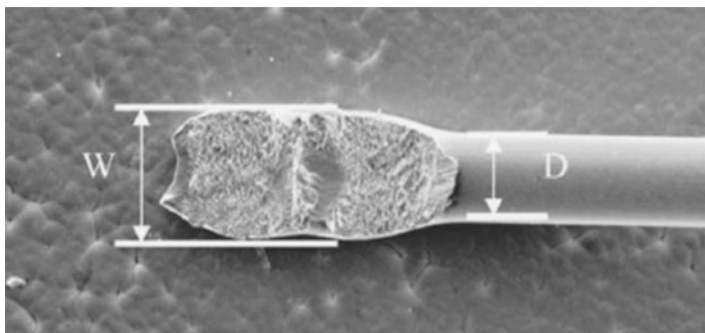


Fig. 7.12 Deformation ratio (D/W) [245]

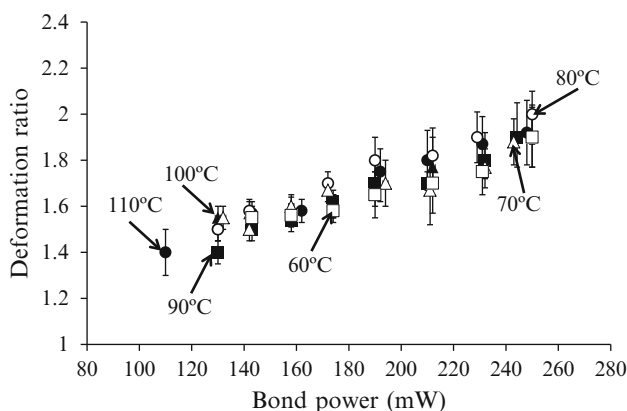


Fig. 7.13 Bond deformation ratio vs. bond power [245]

a response variable to optimize the bonding process. It was found that the deformation ratio decreased with the plasma cleaning due to the reduction in required bond power. For example, when the bond power decreased from 101 to 65 mW, the deformation ratio decreased from 1.25 to 1.2 [245].

When increasing the bond power, the extra energy arising from the higher bond power resulted in deformation of the bond. Figure 7.13 shows how increasing the bond power can increase the deformation ratio, thus weakening the neck of the wire and causing a decrease in pull strength [245].

There was no effect of plasma power or time on the bond pull strength for bond pad temperatures in the range of 60–100 °C at 100 and 400 W (Figs. 7.14 and 7.15, respectively). However, a low power of 100 W was found to be more desirable for achieving a wide bonding process window than a high power of 400 W. Atomic force microscope (AFM) surface analysis indicated that a longer plasma time (5 min vs. 1 min) is detrimental to bond pad cleanliness, as the oxygen plasma reacts with epoxy-based materials, causing contamination of bond pads. Based on

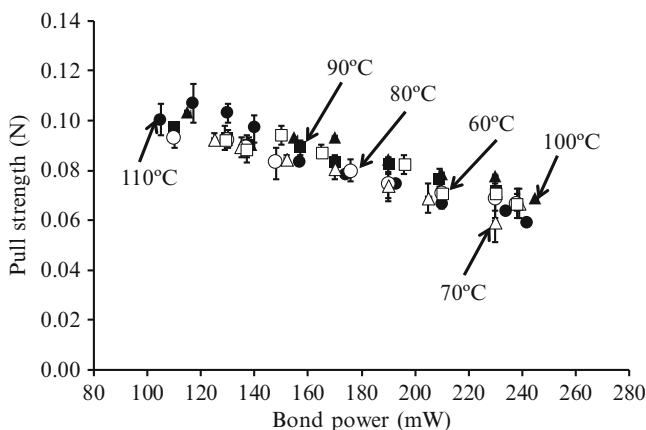


Fig. 7.14 Pull strength data after plasma cleaning with power 100 W: time = 5 min [245]

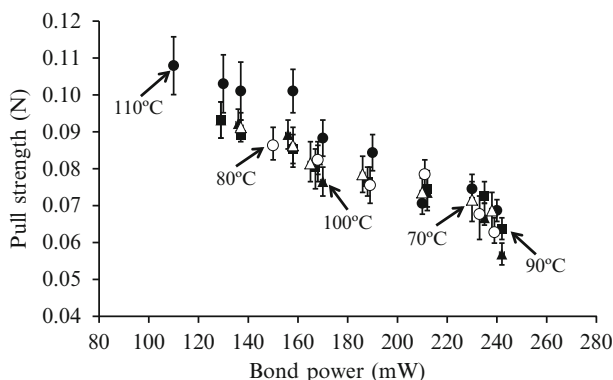


Fig. 7.15 Pull strength data after plasma cleaning with power 400 W: time = 5 min [245]

these findings, low plasma power with low exposure time is desirable for optimal cleaning.

The exposure time after plasma also affects the condition of the bonding surface. It was found that the effect of plasma on the pad surface quality decreased after 1 h of exposure in ambient air, and the contact angle increased from about 8–10° to 20–30° [245]. After 8 h, the contact angle increased to 60°, indicating that the surface quality degraded with the exposure time. A pull strength test conducted as a function of exposure time verified the trend in the contact angle. A decrease in the pull strength was observed with an increase in exposure time (Fig. 7.16). An increase in the contact angle could be explained by an increase in the C–O functional group (Table 7.4), making the surface more hydrophobic [245]. Detection of the functional group was conducted using X-ray photoelectron spectroscopy (XPS).

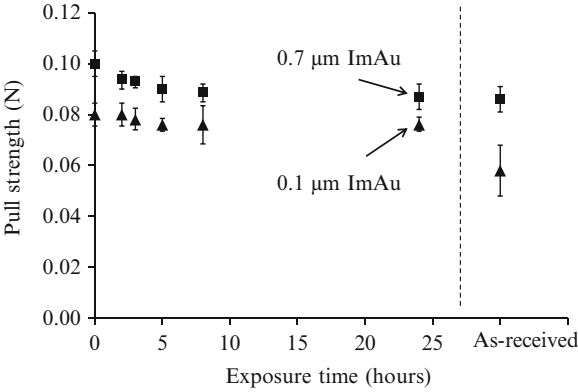


Fig. 7.16 Pull strength as a function of exposure time in air for 0.1 and 0.7 μm Au-finished pads [245]

Table 7.4 Functional groups on the pad surface as a function of exposure time [245]

Exposure time after plasma cleaning (h)	C–H (%)	C–O (%)	O–C=O (%)
As-received	54.6	39	6.3
1	74	15.4	10.6
8	66.5	23.3	10.1
24	63.4	27.5	9.1

Table 7.5 Optimized plasma conditions

		Optimum	High	Risk
Power (W)	–	100	400	Pad damage
Plasma time (min)	–	1	5	Pad contamination
Plasma gases	Argon and oxygen; argon and hydrogen	Minimize oxygen level		Oxides cause parametric shift in devices
Post-plasma exposure time (h)	–	<1	>1	Degradation of pad surface: decrease in pull strength

Table 7.5 lists the optimized plasma conditions for bond pad surface cleaning. The conditions include plasma power, plasma gases, and post-plasma exposure in air.

7.6 Summary

This chapter discussed the common pad materials for wire bonding. The over pad metallizations were also discussed. The wire bonding industry uses Ni-based finishes to facilitate wire bonding with Cu. NiPdAu finish has outperformed aluminum pad metallizations in both shear testing and pull testing. After comparing the

different thicknesses of Ni, Pd, and Au on bond pads, no difference in their reliabilities has been observed. Research on NiPdAu pad finish has also shown that there is not a reduction in shear strength after 2,000 h in high-temperature storage. The industry, however, needs to address the challenges associated with Ni-based finishes, such as developing standardized plating methods, having a reduced capillary lifetime, and having a longer mean time between assist than bare Al pads.

Wire bond strength, bondability, and quality are dependent on bond pad characteristics such as the surface roughness and surface condition (e.g., cleanliness, oxidation level). Cu-low- k structures have been adopted by the semiconductor industry for back end of the line interconnects in an integrated circuit (IC). Cu wire bonding on Cu-low- k structures is a concern for the underlying circuitry due to bonding of a hard metal (Cu) on a hard metal (Cu), as well as the propensity of Cu to oxidize. One approach to address these concerns is to protect the Cu pad with various coatings. Different oxidation protection layers, such as gold, aluminum, and thin inorganic films, have been developed. A second approach is to clean the Cu pad surface prior to bonding.

This chapter also discussed the effects of contaminants, surface oxide films, surface roughness, and plasma treatment on wire bond strength, bondability, and quality. Contamination on the pad surface decreases the quality of the formed bonds, and, hence, decreases the bond strength. Contamination can originate from plating baths, outgassing of materials such as solder mask and adhesives, and the bonding atmosphere. Contamination was also found to originate from packaging materials, such as the paper placed between wafers to protect the pads. Contamination can deposit several film layers that affect bonding. In particular, oxide films cause bonding defects and poor bond quality. Rough bonding surfaces are less ideal for bonding than smooth surfaces due to the reduced contact area between the bonding wire and the substrate pad. Also, rough surfaces are more prone to contaminant entrapment, resulting in bond failures. To eliminate the surface roughness, surface treatment options such as plasma cleaning are performed to prepare the surface for bonding.

The conversion to copper wire bonding faces several technical challenges. The bonding process has to be optimized, and parameter adjustments for first and second ball bond formation and looping profile are needed. Cu is harder than both Al and Au, thus risking damage to the underlying pad and dielectrics. Another concern with copper wire is its propensity to oxidize, which requires oxidation prevention technology. This chapter summarizes the challenges of Cu wire bonding and the industry solutions to those problems.

8.1 Cu Hardness: Al Splash and Pad Cratering

The wire bonding industry has been using Al bond pads because they are inexpensive and easily wire bondable. It has been reported that a Cu–Al bond is more reliable and has a longer life than an Au–Al bond [156]. Additionally, Cu–Al intermetallics grow at a slower rate than Au–Al intermetallics and have a lower tendency to form Kirkendall voids at the ball bond–pad interface [93, 123, 152, 154]. However, the high stiffness of copper introduces difficulties during bonding to Al or Au surfaces. Pure Cu is about twice as hard as pure Au and is more susceptible to work hardening [208]. A higher bonding force (20–25 % higher than for Au) is required because of the higher hardness and greater work hardening [21, 54]. The deformation associated with wire bonding can increase the hardness of Cu by half. Thus, Cu wire bonding can result in up to 30 % higher pad stress than Au wire bonding [27]. This can cause pad peeling and dielectric cracking [209], and the soft Al can also smear off during bonding along the ultrasonic direction, causing Al splash [78].

High-performance devices are increasingly relying on low- k (dielectric constant (k) < 3 [210]) materials under the bond pads to improve the capacitance, device speed, and signal integrity in Cu interconnects [211]. Since low- k materials are very soft and have low mechanical stiffness, Cu wire bonding can damage the circuitry under pad (CUP). Ultralow- k materials are being used in the semiconductor industry; these materials are produced by incorporating porosity into the existing low- k

materials, which increases the risk of pad damage. While the higher bonding force risks pad and CUP damage, the lower force will lead to nonstick-on-pad (NSOP). Bond over active (BOA) technology is another development for miniaturization of semiconductor devices. It enables the use of a “keep-out zone” underneath the bond pad by moving the devices, ESD circuitry, and power and ground buses underneath the bond pads. The implementation of fine-pitch, low- k , and BOA technology in wire bonding has led to several new metal-lift failure modes such as aluminum cap lift, copper metal lift, and tilted metal lift, which are observed under the ball shear and wire pull tests [212].

Ultrasonic energy is employed in Cu wire bonding to break the surface oxidation of the free air ball (FAB) to improve the interfacial adhesion between the FAB and bond pad, as well as to soften the FAB and increase the bonding interface temperature [60]. As a result of the application of ultrasonic energy during bonding, shear forces add to the already applied normal bonding force. Such shear stress can transmit through the bond pad metallization to the brittle, easily fractured dielectrics underneath, leading to pad peeling and bond failure. Since the ultrasonic energy is applied in the horizontal direction without a vertical bonding force in the area, the contact at peripheral areas is weak. The ultrasonic energy can cause an initial crack in the ball periphery, which can then propagate under high-temperature storage (HTS) as well as under corrosive environments, decreasing the bond reliability [213].

Al splash or Al bond pad squeeze is observed in Cu wire bonding because of the lower flow stress of Al as compared to Cu [60]. Although Cu wire bonds can achieve higher shear strength values than Au ($182.47 \mu\text{N}/\mu\text{m}^2$ vs. $121.64 \mu\text{N}/\mu\text{m}^2$), the amount of Al splash increases linearly with the shear per unit area [59]. Therefore, the shear strength must be limited by the minimum Al thickness under the bond pad (remnant Al). The remnant Al under the Cu bonds is less than that in Au bonds because of the higher Al splash [214]. Remnant Al is required to maintain bond reliability, since remnant Al that is too thin can be completely consumed by the Cu–Al IMC, leading to bond failure [127, 215]. Al splash can damage the fragile dielectrics under the pad and can also result in electrical shorting of the bond pad with adjacent pads when the splash is larger than the pad pitch.

8.2 Process-Related Concerns

Cu wire bonding process optimization is essential for bonding process stability and the portability of machines and materials. Process optimization defines a process parameter window for first and second bond quality. The main requirements for FAB formation are consistency of the FAB and tight tolerance in the FAB sizes. The higher bonding force required for Cu wire bonding than for Au bonding risks damaging the pad and underlying circuitry, as well as shorting the adjacent metallization area by USG displacement due to metal damage of the pad material. For fine- and ultrafine-pitch devices, the requirements for ball placement accuracy are stricter than for low-pitch devices [86]. In terms of yield and MTBA requirements,

Cu wire bonding must be conducted for at least an hour without assist, which requires a wide process window. The main concerns with the Cu wire bonding process are discussed below.

8.2.1 Oxidation Prevention Technology

FAB formation requires the generation of high voltage across the electrical flame-off (EFO) gap, causing a high current spark to discharge and melt the tail of the Cu wire to form a spherical ball. Oxidation must be avoided in order to obtain a symmetrical FAB without deviation in size [60]. Cu oxidation during ball formation inhibits the formation of a spherical ball, which in turn affects the reliability of the first bond. Under high-temperature and high-humidity environments, copper oxidation at the interface of the Cu–Al bonding region causes cracks and weakens the Cu–Al bond. Copper oxidation typically starts at the wire region and then spreads to the upper bonded area and then to the bonding interface with time. Cu oxidation also causes corrosion cracks.

Since Cu oxidizes quickly, Cu FABs need to be formed in an inert gas environment. Oxidation can also occur if the cover (inert) gas flow rate is not sufficiently high to provide an inert atmosphere for the FAB formation [61]. It has been reported that the use of single-crystal Cu wires eliminates the need for cover gas during bonding [62]. Requiring inert gas, such as forming gas, to address the oxidation problem adds complications to the bonding process and results in a narrow process window.

8.2.2 Capillary Mean Time Between Assist and Lifetime

Cu wire bonding requires the modification of capillary material and design to lower the ultrasonic energy to achieve the same ball size control as in Au wire bonding [113, 116, 117]. During second bond formation, higher ultrasonic energy is needed to deform Cu wire, leading to work hardening of the section of the wire where the second bond and wire tail meet. The work-hardened area can snap easily, creating a no-tail or missing-tail condition and causing the bonder to fail its automatic bonding sequence. This, in turn, reduces the time between bonding failures, known as mean time between assist (MTBA). A low MTBA leads to lower machine uptime and productivity, increasing the production costs.

Capillary-related failures reduce the MTBA. The capillary lifetime changes dramatically (from four to two million touchdowns) from Au to Cu wire bonding due to faster wear-out. For Au, capillary lifetime reduction is typically caused by cap clogging, buildup, and dopants in the Au. For Cu, capillary wear-out is the main reason for lifetime reduction. The smooth capillary finish typically associated with Au wire bonding does not work with Cu, since it results in wire slippage during bonding and reduced grip between the wire and the capillary.

8.2.3 Wire Bonding for Specialized Applications

Copper wire bonding has already been adopted in high-volume manufacturing (HVM) for low-pin count, heavy wire packages [18, 246, 247]. Bonding to ultrafine pitch and on low- k wafers requires modifications of the bonding tools and manufacturing process. There are many fine-pitch devices in production [19, 21, 27, 29, 30, 42, 59–61, 64, 73, 76, 104, 115, 132, 142, 146, 150, 209–211, 215, 218, 221, 242, 243, 246, 248–258].

Chylak [246] discussed the challenges for converting to high-pin count (>200) Cu wire-bonded devices. The challenges for fine-pitch bonding are similar to those for low-pin count, including the propensity of Cu to oxidize, the higher hardness of Cu than Au, the requirement of a higher bonding force for Cu, and the corrosive nature of Cu. Cu wire bonding needs to be developed for specialized bonding applications such as bond stitch on ball (BSOB) and reverse bonding, and bonding on stacked and overhang dies.

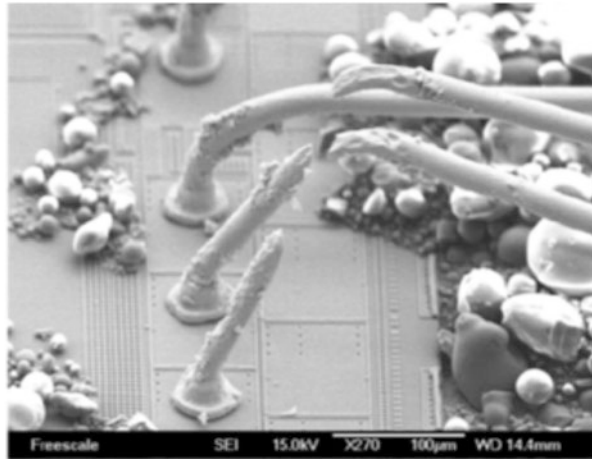
BSOB is performed on extremely low-profile (<50 μm) wire bonding applications. The process consists of a two-step cycle, where a stud ball bump is first formed in the bond pad, and then reverse bonding is carried out. In reverse bonding, the ball bond is bonded onto the lead frame and stitched on top of the ball bump. BSOB with Cu is more challenging than normal Cu bonding due to the multiple bonding impacts on the bond pad [259]. The use of Cu wire induces higher stress in the pad and underlying circuitry than with Au wire due to its high hardness and the strain-hardening effect. Reverse bonding is also an issue with Cu wire bonding because it is difficult to break the wire cleanly due to the higher average elongation of Cu (12 %) than Au (4 %) [177].

Cu bonding on thin overhang dies introduces additional bending and twisting during the bonding process due to the higher bonding force required for Cu than Au bonding [109]. Junhui et al. [111] reported that Cu overhang bonding to a thick Al pad (1.0 μm thick) on a silicon (Si) die leads to greater impact, rebound, and deflection than in a supported die, resulting in lower (~ 0.098 N lower) shear strength of the bond. Additionally, resonance is a risk due to the reduction in the natural frequencies of the stacked die caused by the increase in overhang length. Yen et al. [260] reported that if the die structure exhibits a large amount of vibration at ultrasonic frequency (as in the case of overhung die), it will reduce the ball shear and wire pull strengths of the wire bonds.

8.3 Corrosion from Mold Compound and Decapsulating Chemicals

The mold compound composition requirement for pH and chlorine level is stricter for Cu wire-bonded parts than for Au wire-bonded parts since Cu is highly prone to corrosion from the mold compound [18, 261]. Limited studies on the molding reliability of Cu wire-bonded parts have revealed that Cu wire requires more stringent pH and chlorine (Cl) level control [57, 99, 191, 262] than

Fig. 8.1 Deprocessed copper wire bonds after a wire pull test [156]



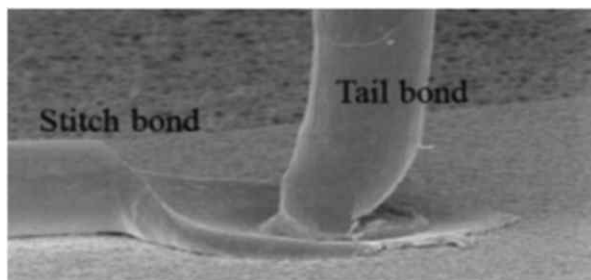
Au wire bonding. Corrosion from the halide ions is observed in Cu–Al IMCs, wherein alumina is formed [29, 262, 263]. The halogen ions re-form, continuing the reaction to form alumina until all the IMCs are consumed, leading to an electrical open. Mold compound suppliers therefore aim to minimize the halogen content in the mold compound [29]. Highly accelerated stress tests (HASTs) are conducted to determine the effect of the mold compound on the reliability of Cu wire bonds.

During the chemical deprocessing or decapping of Cu wire-bonded parts, care must be taken to minimize the possibility of a chemical attack on the Cu wire. Deprocessing is usually conducted with fuming nitric acid or sulfuric acid to remove the mold compound and inspect the wire bonds. These acids cannot be used for Cu wire-bonded parts since they readily attack Cu wire [32]. Severe damage occurs in copper wire bonds during the mold compound removal process, including a reduction in wire diameter. This deprocessed package might not meet the specifications for the wire bond strength tests (shear and pull tests), since the reduction in wire diameter will reduce the pull and shear strengths. Figure 8.1 shows the wire pull test results of a deprocessed copper wire bond. Failure occurs at the neck region that was thinned due to the chemical attack.

8.4 Other Concerns

Apart from the concerns listed in the previous sections, there are other concerns with Cu wire bonding related to second and tail bonds, yield, requalification expenses, lack of standardized test methods, and Cu wire bonding capability in the industry.

Fig. 8.2 Second bond: Stitch and tail bonds [51]



8.4.1 Second Bond and Tail Bond

Cu wire bonding has a lower yield than the Au wire bonding. In general, there is a drop of about 10–30 % units per hour (UPH) as compared to the Au wire process [190]. The reduction in UPH is due to the longer bonding time required to bond with Cu wire. The additional time is required because the first bond forms slowly to avoid pad damage, and more time is required to form the stitch bond. The second bond contributes more to the UPH reduction than the first bond, affecting the MTBA and yield of the bond process; therefore, the second bond must be stable and of high quality. The stability and quality of second bond are the key requirements of a wire bond cycle [109]. Figure 8.2 shows the stitch and tail bonds at a second bond.

The second bond process in Cu wire bonding is more sensitive to ultrasonic energy than Au wire bonding due to mechanical fatigue, a rapid increase in plastic stress, and the larger strain hardening of Cu. This makes Cu wire bonding more prone to broken tail and stitch bond failures such as heel cracks. In order to achieve a stable second bond process and target second bond pull value, the aluminum oxide layer at the interface needs to be broken. A robust tail bond is required during second bond formation to hold the wire until the clamp closes to obtain a preset tail length. If the tail bond breaks before the clamp closes, an EFO open or short tail occurs, which increases the MTBA [97].

8.4.2 Yield and Requalification

One challenge for Cu wire adoption is the requalification expense. Since the Cu wire bonding process is relatively new as of 2013, the requalification expenses for the process and wire-bonded parts are high. The electronic companies are calculating the total cost of the conversion to Cu, which also includes the cost of requalification. Solutions to improve yield and qualify Cu need to be developed.

8.4.3 Lack of Standardized Test Methods and Reliability Data

Owing to the fast-paced transition to Cu, reliability and qualification tests have not been verified for Cu wire bonding, and the industry has adopted the same test methods for Cu as for Au. A database of reliability and qualification test data has to be established before Cu wire bonding can be widely adopted, especially for automotive and critical applications such as military and aerospace.

8.4.4 Lack of Widespread Cu Wire Bonding Capability

The initial cost of the transition to Cu wire bonding is high due to the changes in the equipment, process, and materials that are required for Cu wire bonding. Additionally, the Cu wire bonding equipment, process, and materials have to be optimized to achieve portability between machines and materials. With the exception of a few big wire bonding companies, the rest of the industry does not have the required funds for the transition to Cu wire bonding to achieve high throughput and yield.

8.5 Solutions

This section discusses industry solutions for Cu wire bonding, including optimization of the bonding process and EFO parameters, oxidation prevention technology, solutions for pad cratering, Al splash, surface contamination, mold compound requirements, deprocessing schemes, and improved bonding tools.

8.5.1 Bonding Process Optimization

The process window for Cu wire bonding is narrower than that for Au wire bonding [29]. A good process window for Cu wire bonding can be achieved by designing an experiment that is tailored to the Cu wire bonding process. Bond parameter optimization is aimed at carrying out bonding with no pad cratering or cracking, and 100 % ball bond containment within the pad that is lower than the surrounding metal. Tight capillary control is required to reduce the variation in ball size and facilitate HVM. Another part of process optimization is to obtain adequate IMC coverage [99, 100]. In order to maintain yield, the pad metallization should be cleaned using plasma cleaning to prevent the ingress of foreign particles on the die and substrate prior to bonding.

Process optimization ensures bonding process stability and defines a process parameter window for first and second bond quality [101]. Researchers have adopted several methods for process optimization of Cu wire bonding such as Taguchi methods [102], Six Sigma “define–measure–analyze–improve–control” (DMAIC) methodology [103], orthogonal response surface methodology (RSM) [91, 104, 105], and statistical design of experiments (DOE) [105].

Su et al. [102] demonstrated the application of Taguchi methods for process optimization and increased the yield from 98.5 to 99.3 %, saving USD \$700,000. Lin et al. [103] used the Six Sigma DMAIC methodology to optimize the material, machine, and bonding parameters, developing a new bonding method of flattening the bonded ball and applying gentle ultrasonic operation. They also reported that the capillary design and surface roughness improved the wire bond response. Wire coupling with optimum electrical firing parameters and air cushioning can help to achieve robust and oxidation-free FABs.

Researchers [91, 105] have conducted statistical DOE and RSM on common bonding process parameters, such as contact velocity (C/V), bond power, bond force, USG current, and bonding time, to determine the factors affecting the process. Jiang et al. [91] investigated the process window development for Cu wire bonding based on contact velocity, initial force, bond force, USG current, and bonding time. The DOE was carried out based on those input factors, and the response factors were wire pull strength, ball shear strength, and cratering performance on bond pads. The DOE study adopted a half fractional DOE with the five input factors to look for factors affecting the model. Based on the results, three factors were chosen for advanced DOE with RSM to obtain the final optimum parameter range. Wong et al. [105] conducted DOE to optimize the process parameter window to achieve a ball bond with targeted bonded ball diameter (BBD), bonded ball height (BBH), wire pull, and ball shear strength. The DOE was conducted on bond power, bond force, and bond time to determine the “significant parameters” affecting the process parameter window. The response surface comprised BBD, BBH, wire pull, and ball shear strengths. After the initial screening, full factorial design to determine the interactions between the two significant parameters, bond power and bond force, was conducted. The RSM matrix was used to determine and model the optimum region. Based on the study, bond power was found to be the critical factor in reducing BBD.

In addition to bonding parameter optimization, process control for Cu wire bonding manufacturing conditions has to be conducted. Teck et al. [107] conducted a wire floor life control study to determine the usable life of Cu wire after unpacking it from a wire supplier’s seal with inert gas. The capillary touchdown limit for a 47 μm bond pad pitch with a wire size of 20 μm was determined. Capillary degradation started at 200k touchdowns, and buildup at the capillary sidewall started at 300k touchdowns, causing short-tail conditions. Staging on a heater block was also studied to determine the reliability and manufacturability due to substrate outgassing during wire bond heating. The die-bonded unit was staged on top of the wire bonder heater block for 0, 15, and 30 min to simulate a scenario where a unit was left on a wire bonder heater until the machine stopped. It was found that substrate outgassing did not affect the manufacturability. The wire pull and ball shear strength showed a reduction after 15 min of staging, but an improvement after 30 min of staging. The improvement was attributed to the interfacial IMC growth due to 30 min of heating at 170 °C. Another way to improve the adhesion of Cu–Al after bonding is to enhance intermetallic growth by heat treatment [108].

Process optimization can improve the bond reliability of specialized die structures such as overhang dies [109, 110]. Kumar et al. [109] demonstrated the process characterizations of different overhang die configurations, where a process was developed for consistent ball shape, remnant Al underneath the bonded ball, and looping across the overhang area. Li et al. [111] developed an approach to reduce the bonding impact on the die by increasing the thickness of the Al pad from 1 to 2.8 μm . The micro-hardness of the bond pad structure decreased by three times, leading to a reduction in the impact and rebound force. The shear strength of Cu wire overhang showed an improvement in the shear strength.

In the process optimization approach followed by K&S, a model-based response-driven approach is adopted, wherein a numerical model is derived from extensive process testing, and bonding parameters are scaled for ball diameter. In order to develop the pitch model for Cu wire bonding, the target ball diameter is set and the bonding accuracy and Al splash are taken into account. After this, the wire size is chosen. Cu is 2.54 μm thinner than Au for the same pitch because of Al splash.

The requirements to achieve quality first and second joints are optimized process parameters, an optimal bonding environment, a contamination-free surface, and proper maintenance of the tool MTBA. The bond pads on an active circuit or CUP can be damaged if the bonding parameters are not optimized. The main challenges, as mentioned in Sects. 8.1 and 8.2, are hardness and oxidation. The bonding process needs to be optimized, and parameter adjustments must be made for power, pre-bleed energy, ultrasonic generator (USG) current, EFO current, force, and temperature for the Cu wire bonding process. The optimum power should be determined to achieve good bond quality. With increasing ultrasonic power, shear, but not diameter, should increase. The optimum USG current should be established to achieve a uniform ball bond, as the ball deformation and ball shear force increase with an increase in USG current.

8.5.2 Oxidation Prevention Technology

The oxidation of Cu is prevented in two ways: use of an inert gas (nitrogen or forming gas) during bonding, and use of oxidation prevention coating on Cu wire [42, 63, 64]. The use of N_2 as the cover/shielding gas has resulted in defective FABs. Since forming gas contains 5 % H_2 (95 % N_2 , 5 % H_2), it has better anti-oxidation properties than N_2 and is the cover gas for Cu wire bonding. The main purpose of injecting forming gas (FG) is to form an inert gas shroud around the copper tail and the FAB to prevent oxidation prior to bonding. The use of H_2 has the twofold purpose of helping to melt the Cu, as well as acting as a reducing agent to reduce the copper oxide back to Cu [60].

The use of oxidation-resistant coatings is another way to address the problem of Cu oxidation. Al-coated Cu wires for room-temperature wedge-wedge bonding have been shown to suppress oxidation and to have better pull strength, better

metallic contact formation, and better storage capabilities than bare Cu wires [47]. Al-coated wire is suited for room-temperature bonding on low-temperature co-fired ceramics with silver and gold metallization.

Among the oxidation prevention coatings (Au, Ag, Pd, and Ni), Pd coating on Cu has shown sufficient potential to replace Au wire for its excellent bondability and reliability at a relatively low cost [48–53]. Pd is a semi-noble metal with similarities to both Ag and Pt. PdCu is oxidation free, and Pd has good adhesion to Cu wire and higher tensile strength than bare Cu wire when bonded on Al pads.

Robustness in the second bond is the main reason for adopting PdCu wires [52, 55]. This robustness has led to an improved C_{pk} (process capability index). The stitch pull strength of PdCu wire is more than 50 % higher than bare Cu [51]. PdCu wire on an aluminum bond pad has also been demonstrated to perform better than bare Cu in high-humidity conditions, such as in the highly accelerated stress test (HAST), pressure cooker test (PCT) [50], temperature cycling test (TCT), and HTS test.

Since PdCu wire has a larger diameter than bare Cu wire, the FAB diameter for PdCu wire needs to be smaller than that for bare Cu wire. Because of the Pd layer on the Cu wire, there is always a layer of Pd or a Pd-rich phase that protects the bonded ball from an attack of corrosion. The use of Pd may also ease the stringent molding compound requirement. Pd prevents the formation of CuO and can form a bond with N_2 without requiring forming gas. A comparison of N_2 and forming gas for PdCu wire (15 μm) showed that forming gas is superior to N_2 , since it is not sensitive to changes in EFO (FAB diameter relative standard deviation: 0.94; ball-to-wire offset: 0.53 μm) [57]. Comparisons of bare Cu and PdCu wire have shown that at a higher EFO current, an FAB with bare Cu wire has higher hardness caused by having smaller grains. Varying the EFO current in PdCu wire causes the hardness of the wire to vary due to the different distributions of the PdCu alloy in the FAB [58].

Although Pd coating prevents the oxidation of Cu, it introduces new challenges for wire bonding. It is 2.5 times more expensive than bare Cu [59] and has a higher melting point than Cu [59]. The industry is thus looking to optimize Pd thickness to reduce costs, decreasing the Pd thickness from 0.2 to 0.1 μm [54]. PdCu is harder than pure Cu and, hence, has a higher risk of pad cracking and damage to the CUP. Pd distribution can affect the reliability of Cu wire-bonded devices, but as of 2013, there is no method to control Pd distribution.

8.5.3 Pad Cratering, Al Splash, and Surface Contamination

Pad cratering can be prevented by selecting the appropriate bond pad metallization, thickness, and structure, and optimizing the bonding parameters [216]. Researchers have adopted several approaches to reduce pad damage, such as increasing the bond pad hardness by doping the bond pads with Si or Cu [123], using softer Cu wire along with optimized bond force and ultrasonic power [27, 30, 73, 209], using harder metallization finishes [23, 57, 115, 217], and using more robust underpad structures.

One way to reduce the ultrasonic bond stresses is to select a softer Cu wire or reduce the ultrasound level [209]. Shah et al. [27] demonstrated that adopting a softer Cu wire resulted in a 5 % reduction in ultrasonic force. Also, a reduction in the ultrasound level caused the ultrasonic force to be reduced by 9 %. It has been reported that by using softer wire along with optimized force and ultrasonic power, 39 % lower pad stress than Au wire can be achieved [73]. Shah et al. [218] also reported that by using a 7–9 % lower ultrasound level, the pad stress can be reduced by 42 %. England et al. [28] optimized the bonding force, and the ultrasonic parameters were optimized at bonding temperatures of 150 and 175 °C. It was found that these increased temperatures resulted in a reduction of the bonding force, which in turn can minimize the occurrence of pad cratering.

Another solution to pad cratering is to modify the chip design for Cu wire bonding by using a robust underpad structure and an optimal Al pad thickness [219, 220]. As mentioned earlier, Cu wire bonding on Cu/low- k structures is challenging because the low- k polymers are encased in brittle diffusion barriers that can crack during bonding. Special underpad support structures need to be designed [221]. Chen et al. [220] recommended using an Al layer thicker than 0.8 μm to prevent damage to the pad structure. For Al thicknesses below 0.8 μm , the underpad structure and via distribution need to be optimized to prevent damage to the pad structure. England et al. [219] conducted a study on the influence of the barrier layer structure and composition on the presence of pad cratering, and the use of titanium nitride (TiN) as the barrier layer resulted in a high occurrence of cratering. Pad cratering was absent in Ti and titanium tungsten (TiW) barrier metals, as well as in the configuration of TiN on top of Ti. Periasamy et al. [222] developed hybrid structures using the bottom 2–4 stacks as Cu–low- k and the top 2 stacks as Cu/SiO₂. This structure addresses the problems of bond pad peeling, bond pad sinking, low ball shear, and damage to the underlying circuitry.

The performance and reliability of the Cu wire bonding process can be improved by understanding the microstructural and mechanical properties of FABs and the Cu–Al interface. Researchers have developed several methods, such as nanoindentation and atomic force microscopy, to measure and characterize the hardness of the FAB and the bonding wire [151]. Fan et al. [151] characterized the tensile properties of Cu wire before and after the EFO process by conducting pull tests. The hardening constant in the Hall–Petch equation, which determines the localized stress in the pad, was obtained. The measured material properties provided the inputs for the FEA model to characterize the dynamic response of Cu wire bonding on the Al pad [135, 211, 223].

Pads that are too thin or too thick are undesirable. A pad that is too thin cannot protect the CUP, whereas a thicker pad can have more Al splash and a higher risk of passivation cracks and pad shorts. Damage occurring during wafer probing should be examined since probing might crack the dielectric layer under the pad. A few unbonded devices should always be etched to see if cracks are present.

The industry is exploring options to protect the underlying structures, such as harder pad metallizations. Ni-based finishes are gaining popularity for copper wire bonding. Nickel is about 50 % harder than copper and four times harder than

aluminum, so it provides greater protection against the higher stress resulting from Cu ball bonding, as well as damage during probing. This is especially beneficial for devices with low- k active circuitry under the bond pad [23, 57, 115, 217]. Ni-based finishes have the advantages of high reliability, high bonding load, protection of fragile structures, compatibility between probing and bonding, and compatibility with Au and Cu wire bonding. Typically, a layer of Ni 1–3 μm thick is deposited on either the Al or the Cu base metallization as the surface finish.

A Ni layer by itself is not easily wire bondable because it forms a layer of surface oxide, which is hard and unbreakable. Therefore, a thin noble layer of Au and/or Pd is required on top of the Ni for more robust manufacturability, bondability, and reliability. Typical thicknesses are 0.03–0.05 μm Au, 0.1–0.3 μm Pd, and 1–3 μm Ni [58]. Au provides an excellent bondable surface, but it is an expensive metal. Therefore, owing to cost considerations, the electronics industry is considering several options, such as a palladium layer between the nickel and gold or pure palladium. The use of palladium thins down the Au layer and improves the corrosion resistance of the nickel layer. The diffusion of Ni, Cu, or Au into Pd is slow; therefore, it provides highly reliable bond-pad interfaces. Additionally, Ni-based pads such as NiAu, NiPdAu, and NiPd have good reliability and no Al splash. NiPdAu pad metallization can be applied on both the existing pads and the Cu conductors in semiconductor dies. The finish for laminate pads should be determined based on operating environments, reliability, and cost analysis. Bare Cu wire bonding on NiAu laminate pad finish has been used in the industry due to its good reliability performance. Due to the prohibitive cost of Au, ENEPIG finish is also gaining momentum as an alternate finish for bare copper bonding. Other finishes, such as ImAg, have been shown to be susceptible to corrosion-related failures and are thus not gaining popularity [230]. However, the application of Ni-based finishes is difficult, and the industry is struggling to develop plating processes for these finishes. Capillary lifetime is another issue with Cu wire bonding, especially for Ni-based finishes. Ni and Pd are hard, so it is difficult to bond onto them. The yield decreases from 1 to 2 million bonds per capillary on Al pads to 100 to 200k bonds per capillary for Ni-based pads. Cu wire can also be bonded on NiPdAu-Ag-plated and roughened NiPdAu-Ag-plated lead surfaces, although Li et al. [230] reported that packages with NiPdAu-Ag-plated lead frames showed delamination at the top of the die paddle after stress testing, while packages with roughened NiPdAu-Ag-plated lead frames showed positive results after stress testing.

Al splash can be reduced using several methods. First, high-purity Cu wires can be used. Srikanth et al. [44] reported that higher purity wires have lower flow stress than lower purity wires due to having fewer grains. Because of the lower flow stress, a lower bonding force is required, which results in a lower Al splash. Second, a modified capillary design can reduce Al splash by allowing a lower ultrasonic power than the original design [216]. Third, the ball size can be reduced relative to Au to allow for splash. For many processes, shear and area show a direct correlation. To allow for splash, the ball size must be reduced, which in turn reduces the size of Cu wires required [104, 215]. In general, Cu wires are made 2.54 μm thinner than Au wires. A special process, such as ProCu developed by K&S [54], is

Table 8.1 Loop height of Cu wire and Au wire [265]

Loop height (μm)		
Wire	Gold	Copper
Maximum	59.5	60.0
Average	56.7	56.7
Minimum	52.0	53.0
Range	7.5	7.0
Std. Dev.	2.10	1.74

required for Cu to reduce the splash while still maintaining the shear per unit area. Finally, the Cu wire ball and pad can be made to rub against each other in a direction intersecting the ultrasonic wave application direction, minimizing Al splash [224].

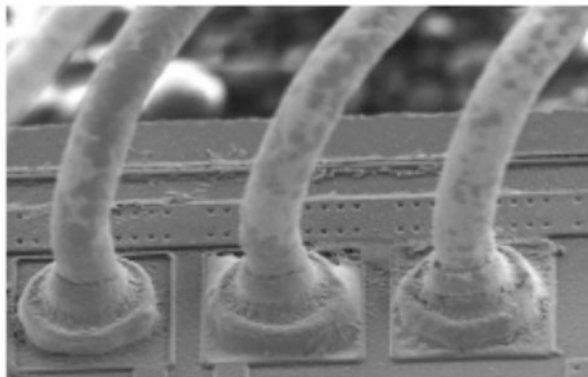
Wire bond bondability and quality depend on the quality of the bond pad surface. The presence of contamination on the bond surface affects the formation of quality bonds, and, hence, bond strength. Plasma cleaning has been found to remove organic contaminants from the surface of the bond pad [245]. Plasma cleaning used in conjunction with optimized wet and dry cleaning processes cleans the surface before bonding. The primary gases used for plasma are oxygen and argon.

Loop height in stacked die packages, especially for ultrafine-pitch applications, must be optimized. In order to avoid electrical shorting between different loop layers in stacked packages, the loop height must not be greater than the die thickness [264]. Compared to Au, Cu requires extra shaping to make the desired loop shapes. Cu wire is less prone to wire sway and has better mold sweep properties. Hence, the process parameters for looping are different. Since the tail bond affects MTBA, it is necessary to obtain a balanced process and form a tail bond without affecting the looping. It has been reported that with proper parameter optimization, the loop height of Cu wire can be comparable to that of Au wire (Table 8.1) [265].

8.5.4 Mold Compound and Deprocessing Scheme

Cu corrosion from the halides in the mold compound can be prevented by the choice of mold compound [29, 99, 262, 263, 266]. Mold compound suppliers aim to minimize the halogen content in their mold compounds by screening the resins for low halogen content, adding additives as ion trappers [267], buffering the pH (buffer solutions are used to maintain the pH at a near-constant value), and modifying the glass transition temperature [29]. Abe et al. [267] developed a new ion trapper through chemical model simulation, which was shown to pass 336 h at 130 °C/85 % RH/5 V with bare Cu wire. The Pd layer in the PdCu wires acts as a barrier layer for Cl⁻ penetration, potentially behaving as a Cl⁻ catcher.

Fig. 8.3 A chemically deprocessed Cu wire package showing no damage to the copper wire [57]



“Green” mold compounds and substrates are materials that do not include bromine (Br) or antimony (Sb), both of which have been identified as being environmentally hazardous. Green mold compound and green substrate (both with low halide content) with optimized wire bonding parameters improve the reliability performance of Cu wire bonds and help in minimizing and mitigating the copper ball bond corrosion under uHAST or THB reliability tests [263]. Seki et al. [262] reported that HAST conditions (140 °C, 85 % RH, and 20 V for 480 h) for Cu wire-bonded devices can be improved by combining a pH buffer and epoxy with low Cl ions. Additionally, some FRs have a negative impact on HAST performance. The use of aluminum hydroxide and green epoxy molding compound (EMC) without flame retardants exhibited good HAST performance, whereas the HAST properties of EMC with magnesium hydroxide ($\text{Mg}(\text{OH})_2$) are inferior to those of EMCs with aluminum hydroxide ($\text{Al}(\text{OH})_3$) owing to the high pH of $\text{Mg}(\text{OH})_2$ [262].

The deprocessing recipe should be optimized for the copper wire-bonded packages in order to prevent damage to the copper wire. As seen in Fig. 8.3, a good deprocessing recipe prevents chemical attack on the copper wires [57]. Murali et al. [268] recommended a mixture of fuming nitric acid and 96 % concentrated sulfuric acid for decapping the epoxy encapsulation in Cu wire-bonded packages. Other techniques of decapsulation are laser ablation and plasma etching [269], and each of these techniques has its inherent advantages and disadvantages. Tang et al. [269] provided a review of these techniques. Laser ablation employs a laser beam to ablate the mold compound and create a uniform opening in the plastic packages. However, the laser can cause damage to the die and thus is recommended as a pre-decapsulation method. Plasma decapsulation has the advantage of high etching sensitivity, but is slow in removing the silica fillers in the mold compound. This in turn reduces the etching rate. Plasma ions may also cause damage to the IC package. Tang et al. [269–271] demonstrated the decapsulation of Cu wire-bonded plastic packages by using atmospheric pressure microwave-induced plasma (MIP). This has several advantages: the etching rate is at least ten times higher than the conventional plasma etching, localized etching, and localized heating;

hence, damage to the IC is prevented, potential electrical damage caused by RF field is reduced, and a vacuum system is eliminated since MIP operates at atmospheric pressure.

8.5.5 Yield Improvement

The formation of a high-quality second bond is a challenge for Cu wire bonding. The thin oxidation layer on the Cu wire surface makes bonding more difficult than in Au bonding. PdCu wires and special capillaries are developed to mitigate these differences. PdCu wire is adopted because of the robustness in the second bond. The stitch pull strength of PdCu wire is more than 50 % higher than that of bare Cu [51]. The PdCu wires have a higher second bond strength than bare Cu wires, and zero defective second bonds [48]. PdCu also works better at higher USG current levels than Cu wire. It should be noted, however, that due to the higher hardness and rigidity of PdCu over Cu, a higher bonding force is needed for PdCu wires, which could increase the risk of Al splash and pad damage [56]. Hence, careful optimization of bonding parameters is needed for PdCu wires.

Another modification for second bond formation in Cu wire bonding is the use of granular surface tools to minimize wire slippage during bonding and improve gripping between the wire and the capillary [113, 115, 116]. For improved capillary design, considerations such as surface morphology, physical dimensions, and the bonding process window need to be taken into account in engineering evaluations [114]. Goh et al. [113, 116, 117] developed a new capillary design with enhanced capillary tip surface texture, a larger inner chamfer, a larger chamfer diameter, and a smaller chamfer angle for improved bondability. The modified design led to smaller ball bonds, resulting in higher reliability under HTS tests. The granular capillaries used in Cu wire bonding wear out quickly compared to the polished capillaries used in Au wire bonding. Teck et al. [107] studied the capillary touch-down limit for a 47 μm bond pad pitch with 20 μm wire size. It was found that at 200k touchdowns, the capillary started wearing out. At 300k touchdowns, the buildup at the capillary wall resulted in stoppages due to short tail lengths. Therefore, it was recommended that the capillary life of the Cu wire should be controlled at a maximum number of touchdowns of 300k to avoid stoppages.

The bonding force must be optimized for second bonds. Too much force causes nonstick-on-lead (NSOL) and mold flash, whereas too little force does not clean the surfaces sufficiently and results in low stitch strengths. Additionally, plasma cleaning, typically argon plasma cleaning, is performed on all substrates within 8 h of wire bonding [54].

The formation of stitch bonds on quad-flat packages (QFPs) is a challenge for Cu wire bonding. Ultrasonic energy cannot be used for the stitch processes on QFP packages due to the resonant condition of the lead beams that causes wire fatigue and breakage. Thermocompression scrub is used instead, with a combination of force and low-frequency X-Y table scrubbing [54].

For Cu wire bonding on pre-plated lead frames, the low strength of second bonds, which is related to the cold forming (high-speed forging process) of Cu wire, is a challenge. Bing et al. [70] conducted vacuum heat treatment of samples at 200 °C for 10 min, followed by wire pull tests and microstructure observations. Deformed grains in the second bonds went through a recovery process, resulting in the bonding strength of the second bonds exceeding the Cu wire strength.

Cu wire bonding has low UPH because of the longer bonding time for the formation of first and second bonds, compared to Au wire bonding, due to the high hardness of Cu. Mechanical limitations such as heat profile delays, mechanical motion delays, and bonding delays introduce additional delays in the bonding time. Process and bonding time optimization need to be carried out to improve the UPH. Low MTBA is mainly caused by non-sticking and short tail. Appelt et al. [68, 69] reported successful implementation of fine-pitch Cu wire bonding in HVM, where the quality and yield were equal to those of Au wire bonding. Those Cu wire-bonded parts exceeded the standard JEDEC reliability testing specifications by twice the recommended amount.

8.6 Summary

This chapter explained the challenges that need to be overcome in order to facilitate the widespread adoption (automotive, military, and aerospace) of Cu wire bonding. The main concerns with Cu are the hardness and propensity to oxidation. Cu is harder than both Al and Au, causing higher stresses in the underlying pad and die material. Cu wire bonding is not suitable for fragile structures because it requires a higher bonding force than Au. Another concern with Cu wire is its propensity to oxidize, which imposes the additional requirements of an inert atmosphere or Pd-coated wires to prevent oxidation. To address Cu oxidation, bonding is typically carried out in an inert environment, such as in forming gas. Another approach is to adopt Pd-coated Cu wire, which is more resistant to oxidation. Pd can form uniformly shaped FABs with nitrogen instead of forming gas, has better bondability on lead surfaces than Cu wire, and is resistant to oxidation and corrosion. Additionally, PdCu wire forms a robust second bond.

Bonding Cu wire to bare Al pads causes Al splash and can damage the underlying circuitry. Researchers have adopted several approaches to reduce pad damage, including increasing the bond pad hardness by doping the bond pad with Si or Cu, using softer Cu wire along with optimized bond force and ultrasonic power, and using hard metallization finishes. The industry is exploring Ni-based finishes to address the problems caused by the high hardness of Cu. Nickel-based bond pads, such as NiAu, NiPdAu, and PdAu, address the issues of high hardness, high yield strength, and high required bonding force in Cu wire bonding, since Ni is several times harder than both Al and Cu. However, Ni-based pad finishes are difficult to implement and reduce capillary lifetime. Another solution to pad damage is to modify the chip design for Cu wire bonding to obtain a robust underpad structure

and to use optimal Al pad thickness. Al splash can also be reduced by using high-purity Cu wires, modified capillary design, and thin wires.

Cu bonding requires a granular capillary finish to prevent slippage between the capillary and the bond pad. However, the granular finish reduces the capillary MTBA and lifetime due to faster wear (especially during second bond formation), compared to the smooth capillary finish. As of 2013, there are no standardized tests for Cu wire-bonded devices, and it is unknown whether the tests designed for Au wire-bonded devices are sufficient to qualify Cu wire-bonded devices. Cu has more stringent requirements than Au regarding the mold compound in molded packages due to its sensitivity to pH and chlorine content. Process optimization and parameter adjustments for ball bond formation, stitch bond formation, and looping profile are needed as well.

Wire bonding with copper wire has become widely accepted as an alternative to wire bonding with gold wire. Because Cu has a higher thermal and electrical conductivity and lower cost than Au, it has been used as a replacement for conventional Au wire and is gaining acceptance in consumer electronics. However, Cu wire bonding also has limitations and pitfalls. The propensity to oxidize, high hardness and yield strength, and susceptibility to corrosion are the main disadvantages of Cu wire. Due to the cost savings involved in using Cu, the industry is continuing to move towards Cu wire bonding. This chapter provides specific recommendations for the Cu wire bonding process.

9.1 Copper Wire Bonding Process

The Cu wire bonding process needs to be optimized in order to address the concerns of high hardness, oxidation, and corrosion sensitivity of Cu. In order to address Cu wire oxidation, two approaches have been adopted in the industry: conducting bonding in an inert environment such as forming gas (95 % N₂, 5 % H₂), and using palladium (Pd)-coated Cu wires. Although an inert atmosphere provides a solution to the problem of Cu oxidation, the use of PdCu wire is a preferred solution for oxidation because it achieves a wider process window and forms a reliable second bond. Since Cu wire is harder than Al, it causes lateral displacement when bonded on an Al pad, which can damage the fragile dielectrics under the Al pad. Nickel (Ni)-based pads are a potential alternative to bare Al pads, since Ni is harder than both Al and Cu. Another approach is to make the underpad structure stronger so that it can withstand the high bonding force without damage.

The bonding process must be optimized to minimize defects and form a reliable joint. During thermosonic bonding, heat softens the bonding wire and board metallization. The wire softening is also achieved by adjusting the power and time of the ultrasonic energy. The optimum power should be determined to achieve good bond quality. Insufficient power has been shown to result in under-formed bonds and tail lifts, while excessive power can result in damaged joints. Other

parameters for bonding process optimization include EFO current and firing time, bonding force and temperature, and cover gas flow rate. FAB formation requires the generation of high voltage across the EFO gap, causing a high current spark to discharge and melt the tail of the Cu wire to form a spherical ball. The heat-affected zone (HAZ) length is directly proportional to the EFO current and firing time. EFO current and firing time must be minimized to minimize the HAZ in order to increase the ball deformability. On the other hand, with an increase in the EFO current, the arc duration required to form the FAB decreases. The decrease in arc duration, in turn, results in less available time for heat to penetrate axially along the wire away from the ball. The heat penetration along the wire should be minimized since it decreases ball deformability. Hence, an optimum EFO current and firing time have to be achieved to obtain uniform FABs. For PdCu wire, changing the EFO current varies the hardness because of the different distributions of the PdCu alloy in the FAB. The cover gas flow rate also needs to be optimized based on the wire diameter and type of EFO current. A slow flow rate causes an asymmetric shape of the FAB, while a high flow rate results in pointed balls, both of which are unacceptable from a reliability standpoint.

The bonding force also needs to be optimized. An increase in bonding force allows for proper coupling of ultrasonic energy between the bond wire and pad metallization. A high bonding force transmits high force onto the bond pads, which is not desirable, since it can damage the pad or cause pad cratering. On the other hand, a low bonding force leads to the nonstick-on-pad (NSOP) condition.

With regard to the copper wire bonding process, we make the following recommendations:

1. An inert atmosphere must be provided to surround the FAB and prevent oxidation. Bonding is typically conducted in inert forming gas (95 % N_2 , 5 % H_2) to prevent the oxidation of Cu wire.
2. The micro-hardness of bonded Cu balls is related to the EFO parameters, with the hardness of FABs being inversely proportional to the EFO current. This lower hardness is attributed to the higher maximum temperature during FAB melting due to the high EFO current. Because EFO current and EFO firing time are closely related, it is more appropriate to use firing time as a hardness index for FABs than to use EFO current. For Cu wire bonding, to achieve a soft FAB and minimize the stress induced during ball bond impact, it is recommended to have a shorter firing time during FAB formation, use a lower contact velocity to minimize the impact stress, and use a higher gas flow rate to provide sufficient inert gas coverage to avoid pointed FABs.
3. The ratio of bonded ball volume to FAB volume should be considered when moving from Au wire bonding to Cu bonding. A Cu FAB should be made smaller than a Au FAB, or else it will result in a higher ball bond and a weak joint.
4. Due to the high bonding force involved in Cu bonding, if using an Al pad, the process must be optimized to minimize Al splash, which is an undesirable feature that can result in package failure. One of the ways to accommodate Al splash is to use thinner ($\sim 1\text{ }\mu\text{m}$ thinner) Cu wires. Another way to reduce bond

pad stresses is to reduce the ultrasonic bond stresses by selecting a softer Cu wire or reduce the ultrasound level. Another solution is to modify the chip design for Cu wire bonding. The main factors in chip design are robust underpad structure and an optimal Al pad thickness. Special underpad support structures need to be designed for Cu wire bonding to protect the low-k polymers encased in brittle diffusion barriers.

5. Second bond formation is a challenge with Cu wire bonding due to the tendency of Cu to oxidize; granular surface tools should be used to minimize wire slippage during bonding and improve gripping between the wire and the capillary. For improved capillary design, considerations such as surface morphology, physical dimensions, and bonding process window need to be taken into account in engineering evaluations.
6. Cu corrosion from the halides in the mold compound can be prevented by minimizing the halogen content in the mold compounds by screening the resins for low halogen content, adding additives as ion trappers buffering the pH (buffer solutions are used to maintain the pH at a near-constant value), and modifying the glass transition temperature of the mold compound.
7. During the chemical deprocessing of Cu wire-bonded parts, the possibility of chemical attack on the Cu wire should be minimized. If left unchecked, this could completely remove the wires or reduce the wire diameter significantly. The deprocessing recipe should be optimized for the Cu wire-bonded packages in order to prevent damage to the Cu wire. A mixture of fuming nitric acid and 96 % concentrated sulfuric acid is one of the recipes for decapping the epoxy encapsulation in Cu wire-bonded packages. Other techniques of decapsulation are laser ablation and plasma etching, and atmospheric pressure microwave-induced plasma (MIP).

9.2 Palladium-Coated Copper Wires

The use of bare Cu is a concern due to the propensity of copper to oxidize. Cu oxidation reduces bondability of wire and is also known to cause corrosion cracks. Coating the Cu wire with Pd offers a solution to prevent Cu oxidation during the bonding process. Pd has good adhesion to Cu wire and higher tensile strength than bare Cu wire. PdCu is oxidation free, and the second bond pull strength of PdCu wire is more than 50 % higher than bare Cu. PdCu wire on an Al bond pad performs better than bare Cu in high-humidity conditions, such as in the highly accelerated stress test (HAST) and the pressure cooker test (PCT) [157, 194]. The robustness of the second bond has led to an improved process capability index (C_{pk}). Because of the Pd layer on the Cu wire, there is always a layer of Pd or a Pd-rich phase that protects the bonded ball from an attack of corrosion. The use of PdCu wire also eases the stringent molding compound requirement in Cu wire bonding. Pd prevents the formation of CuO and can form bonds with N₂ instead of requiring forming gas. Bond strength studies of PdCu wire on Al pads indicate that the first bond pull strength is about 11 % higher for PdCu wire compared to Cu wire [51]. However,

when exposed to high temperature at 175 °C, the joint strength for PdCu wire was found to degrade after just 24 h at 175 °C. This decrease in bond strength was attributed to the diffusion of Pd at the interface after high-temperature aging [51]. Although Pd coating offers an alternative to prevent the oxidation of Cu, PdCu wire is 2.5 times more expensive than bare Cu. The industry is thus looking to optimize the Pd thickness to achieve cost-reductions, and the Pd thickness has come down to 0.1 μm from 0.2 μm .

The recommendations for PdCu wires are as follows:

1. Pd distributions should be analyzed in the copper wire itself, the FAB, the bonded ball, and the bond-pad interface using scanning electron microscopy (SEM) and electron-dispersive microscopy (EDS).
2. A series of experiments and shear and pull tests should be conducted to investigate the influence of Pd coating on the strength of Cu wire-bonded parts.

9.3 Bonding Pad

The bondability and reliability of a wire bond depend on the quality of the bond pad surface. Contamination on the pad surface reduces the quality of bonds and reduces the bond strength. Rough pad surfaces are less ideal for bonding than smooth surfaces due to the reduced contact area between the bonding wire and the substrate pad, and they are more prone to contaminant entrapment, resulting in bond failures. Plasma cleaning is used to clean the pad surface before bonding. The primary gases used for plasma are oxygen, argon, and hydrogen.

Reliable and defect-free Cu ball bonding is dependent upon the bond pad, barrier metal, and metallization. Ni-based finishes are gaining popularity for Cu wire bonding. NiPdAu finish has been demonstrated to outperform Al pad metallization in both shear testing and pull testing [217]. In addition, several Ni-based finishes, including Ni/Au, electroless Ni/immersion Au (ENIG), electroless Ni/autocatalytic Au (ENAG), electroless Ni/electroless Pd/immersion Au (ENEPIG), and immersion silver (ImAg), are being investigated by the electronics industry. Using Au on top of the nickel prevents the diffusion of Ni into the Cu. Pd is developed as an intermediate layer between Ni and Au to act as an additional protective layer and reduce the cost of plating. Finishes such as ImAg have been shown to be susceptible to corrosion-related failures and, thus, are not popular [230]. The pad finish should be defined based on operating environments, reliability, and cost analysis. The variations of Cu wire and surface finishes are relatively new. Therefore, it is necessary to assess the pad finish combinations in terms of their manufacturing variability and reliability.

Recommendations for the bond pad finishes are listed below:

1. Due to the higher stiffness of Cu wire than Al, Ni/Au or NiPdAu pads should be used, as opposed to bare Al pads, to minimize pad damage during bonding. Studies should be conducted to determine the reliability of Cu wire bonding on Ni/Au and NiPdAu bond pad metallizations. The effects of pad surface roughness and thickness of metallization layers should be evaluated.

2. Pad contamination decreases the bond strength. An investigation should be conducted on a cleaning procedure and surface preparation prior to bonding. Plasma cleaning is used for removing organic contaminants from the surface. Plasma cleaning should be used in conjunction with optimized wet and dry cleaning processes.
 - (a) The effects of plasma on bonding strength should be investigated.
 - (b) Primary plasma gases for removing contamination, such as oxygen, argon, and hydrogen, should be used with an optimal combination of plasma parameters, such as plasma time, gas mixture, power, flow rate, and operation sequence, to achieve optimal bond strength.

9.4 Bond–Pad Interface

Intermetallic compound (IMC) formation at the wire bond–pad interface is desirable for forming a reliable metallurgical bond. However, excessive IMC formation can be detrimental to the wire bond strength because of its inherent brittleness and propensity to experience voiding.

Cu wire bonding on bare Al pad results in the formation of Cu–Al IMCs. In a Cu–Al system, the larger size difference between Al and Cu than Al and Au, in addition to the lower electronegativity of Cu than Au, restricts the solubility of aluminum in copper, thus forming thinner IMCs as compared to an Au–Al system. Additionally, extensive Kirkendall voiding has been observed in Au–Al IMCs [122, 158, 161], whereas very sparse Kirkendall voiding has been observed in Cu–Al IMCs [124, 126]. Hence, a Cu–Al system has a lower risk of interfacial failures at the ball bond–pad surface interface than an Au–Al system. In order to accelerate the growth of IMCs in a Cu–Al system, 175 °C is used for initial screening. Cu wire bonding on Au-based bond pads results in Cu–Au IMCs. Cu–Au systems do not have voiding below 200 °C up to 100 h of aging. Additionally, IMC growth below 250 °C is sparse, and reliability risks have not been reported below this temperature. Cu wire bonding on pads with different surface finishes results in different bond–pad interfaces. For example, in bond finishes such as NiPdAu and NiAu, the interfacial reaction occurs between the Cu wire and Ni, Pd, and Au. There is no IMC formation for Cu on NiAu or NiPdAu wire bond pads due to the full solubility in the interface combinations of Au, Ni, Pd, and Cu [154].

Microstructural characteristics must be considered to understand the reliability of interconnects. Microstructural features to be investigated include the following:

1. The interfacial IMCs formed under new interface materials should be extensively studied under high-temperature storage (HTS) and TC tests. Metallographic examinations should be conducted to detect voiding, if any. Mechanical and electrical properties of the IMCs, such as hardness and resistivity, should be documented. Shear and pull tests should be conducted on aged specimens to determine if interfacial IMCs play a role in wire bond failure.
2. According to the binary Cu–Au phase diagram, there are three IMC phases—Cu₃Au, CuAu, and CuAu₃—that occur when the temperature is above 200 °C,

with the Cu_3Au IMC layer being visible first. For IMC analysis, an aging temperature of $250\text{ }^\circ\text{C}$ is recommended for analyzing Cu–Au IMC phases.

3. To analyze the IMC formation for a Cu–Al system, an aging temperature of $175\text{--}300\text{ }^\circ\text{C}$ should be used. A Cu–Al system involves the formation of multiple IMC phases, namely, CuAl_2 , CuAl , Cu_4Al_3 , Cu_3Al_2 , and Cu_9Al_4 . After high-temperature aging, CuAl_2 is the first IMC that appears.

9.5 Strength and Reliability Evaluation

Evaluation tests and inspection techniques for wire bonds depend on the application and architectural requirements. Good bonds can be developed consistently with quality controls in process, materials, and design during production. Bonding inspection should be conducted both prior to bonding and after bonding. Bond inspection tests are either nondestructive or destructive. While nondestructive tests yield information about the electrical and quality requirements of joints, destructive tests yield information on long-term performance and package robustness. Bonding pads can be damaged during an electrical probing test, which damages the pads before bonding and leads to defective bonds. Pads should also be checked for level of contamination, oxide formation, and plating chemistry. Several techniques are presented in MIL-STD-883 to evaluate joints and implement process controls to yield good joint quality. Due to the lack of standardized tests for Cu wire bonding, companies such as K&S are adopting their own test methods and target specifications.

Recommendations for wire bond inspection and strength evaluations include the following:

1. During the bonding process, three outcomes are observed: liftoff, sticking, and wedge bond cut due to excessive deformation. Bonding process optimization should be conducted, and the defects arising from bonding should be inspected and avoided.
2. Bond strength should be characterized using the shear and pull tests after different treatment conditions.
3. Three common failure modes observed during pull testing are interfacial breaking from the metallization, wire break at the neck, and bond break. Wire break at the neck is the preferred break mode during the pull strength test. A break of the wire indicates a strong bond between the wire and the metallization.
4. Target specification for pull strength: Minimum of 0.029 N.
5. Target specification for shear strength: Minimum of 0.078 N.

Reliability and quality tests identify failure mechanisms, each of which should be documented and prevented to achieve a robust process and package. Reliability tests with Cu wire bonding include HTS tests, where storage temperature could range from 150 to $250\text{ }^\circ\text{C}$ depending on the bond–pad combination and operating conditions. High-temperature applications with temperatures above $200\text{ }^\circ\text{C}$ require a storage temperature of $250\text{ }^\circ\text{C}$ to accelerate IMC growth and produce interfacial failure mechanisms, while commercial electronics conduct tests at temperatures

around 150 °C to assess the failure-free operation period. In addition, molded packages require reliability tests such as temperature cycling, PCT and HAST (unbiased and biased) to assess performance against moisture, and electromigration. Temperature cycling is conducted to evaluate the reliability implications of flexure resulting from differences in thermal expansion of packaging materials. The failure mechanisms during temperature cycling include flexure failure of the wire at the heel, bond pad–substrate shear failure, and wire–substrate shear failure. Reliability tests should be followed by inspection tests, such as optical inspection, to analyze any bonding damage; a pull strength test and shear test to analyze bond strength; and electrical tests to assess parametric shifts. For PdCu wire, in addition to conducting reliability testing, failure analyses should include locating the Pd presence in the joint, since the interfacial presence of Pd could be the cause of early failures in reliability testing.

Bonds formed by Cu wire on Au pads have been shown to pass reliability tests, including HTS (150 °C) and thermal cycling (1,000 cycles: –40 to 125 °C), with pull strength and shear strength values above the target test specifications (pull strength > 0.029 N and shear strength > 0.078 N) [119]. First bond comparisons of Cu and PdCu wires for unaged (as-bonded) samples have shown that PdCu wire has higher pull strength than Cu wire. However, the bond strength for PdCu wire degrades after just 24 h at 175 °C, also leading to a higher rate of pad peeling failure [51]. This bond pull strength degradation is attributed to the congregation of Pd near the interface. Pd segregates at the interface after extended aging at high temperatures. Comparisons of the second bonds of Cu and PdCu wires on the BGA substrate have revealed that the stitch pull strengths are similar, but PdCu bonds show 50 % higher tail pull strengths than Cu bonds [51]. Cu wire-bonded packages have been qualified against thermal cycling testing, and Cu wire bonds have been shown to pass different temperature cycling test regimes, such as –50 to 150 °C, –40 to 125 °C, and –65 to 150 °C, for up to 1,000 cycles [57, 119, 190].

It has been reported [157, 193] that in high-temperature and high-humidity environments, Cu oxidation at the interface of the Cu–Al bonding region causes cracks and weakens the Cu–Al bonding. Copper oxidation typically starts at the wire region and then spreads to the upper bonded area and then to the bonding interface with time. The reliability of the Cu–Al system can be improved by reducing corrosion through optimization of the bonding conditions and pretreatment of the bond pads. Researchers [157, 194] have evaluated the high humidity reliability of Pd-coated copper wire and found that PdCu wires are more reliable under high-humidity conditions than bare Cu wires. The bond–pad interface for bare Cu wire shows continuous cracking due to chlorine (Cl)-induced corrosion, whereas for PdCu wire, no cracking was observed [194].

Failure mechanisms related to electromigration have been investigated for a Au–Al system [199], but they have not been investigated for a Cu–Al system yet. However, it has been reported that the resistivity of Cu–Al IMCs is lower than that of Au–Al IMCs [200]. Electromigration studies similar to those for Au–Al bonds should be conducted for Cu or PdCu wire on Ni/Au and NiPdAu pads to analyze the effects of high current on IMC formation. The effects of a reversal of current should

also be examined to understand the growth behavior of IMCs under the usage life of electronics.

Recommendations for reliability tests, qualification, and failure analysis include the following:

1. Wire bond–metallization combinations should be qualified under common evaluation and reliability tests such as pull tests, shear tests, visual inspection, corrosion testing, and HTS testing.
2. The wire bond–metallization combinations should also be qualified for a variety of package types under reliability tests such as thermal cycling, shock, and vibration tests.
3. During failure analysis, the location and distribution of Pd should be investigated, as Pd segregation at the bond–pad interface is detrimental to the reliability of PdCu wires. The bonding conditions must be optimized to minimize Pd diffusion into the ball to achieve high reliability.
4. Failure mechanisms in the reliability tests are listed below:
 - (a) Moisture-related failure mechanisms: HAST, uHAST, THB, MSL conditioning and reflow, PCT, autoclave.
 - (b) Corrosion-related failure mechanisms: HAST, THB, PCT.
 - (c) Electromigration: Biased HAST, THB.
 - (d) Electrochemical migration-related failure mechanisms: THB, HAST, uHAST.
 - (e) Package-level failure mechanisms: PCT, HAST, THB, thermal cycling, thermal shock, MSL reflow.
 - (f) Fatigue-related failure mechanisms: Thermal cycling, thermal shock.
5. Reliability monitoring should be conducted using contact resistance measurement techniques and electrical resistance change techniques.
6. Reliability testing should take into consideration the operating conditions and application. For high-frequency applications, reliability tests should measure electrical parametric shifts using a network analyzer.

Appendix A: Reliability Data

Table A.1 Mechanical properties of wire metallurgies [272]

Wire material	Melting point (°C)	Thermal conductivity (W/m K)	Electrical resistance (Ω m)	Young's modulus (GPa)	Tensile strength (MPa)	Hardness at the ball (HV)
Gold (Au)	1,064	315	2.33×10^{-8}	80	240	60–80
Copper (Cu)	1,083	393	1.72×10^{-8}	120	290	80–90
Pd-coated copper	1,083	393	1.80×10^{-8}	120	290	85–95

Table A.2 Electrical properties of wire metallurgies [272]

Bondwire diameter	Frequency DC	Frequency 10 MHz	Frequency 25 MHz	Frequency 75 MHz	Frequency 500 MHz	Frequency 1 GHz	Frequency 10 GHz	L Wire (nH/mm)	C Wire (pF/mm)
<i>R</i> Wire/mm (mΩ/mm)									
20 μm	72.49	72.75	73.29	76.08	129.37	175.50	518.58	0.82	0.06
25 μm	46.48	46.77	47.44	51.33	101.52	138.06	416.80	0.78	0.06
33 μm	27.61	27.94	28.86	34.39	76.53	105.16	324.29	0.73	0.06
Pd-coated copper (conductivity = 5.55×10^7 S/m; <i>R</i> Wire/mm (mΩ/mm))									
20 μm	56.04	56.32	56.92	60.31	112.46	152.55	456.54	0.82	0.06
25 μm	35.95	36.26	37.04	41.71	88.20	120.56	367.86	0.78	0.06
33 μm	21.38	21.75	22.84	29.13	66.85	92.24	287.11	0.73	0.06
Copper (conductivity = 5.8×10^7 S/m)									
20 μm	53.68	53.96	54.58	58.08	109.84	149.06	447.20	0.82	0.06
25 μm	34.45	34.76	35.56	40.36	86.17	117.88	360.31	0.78	0.06
33 μm	20.48	20.86	21.98	28.38	65.37	90.26	281.37	0.73	0.06

Table A.3 First bond USG experimental results for Cu wire [51]

Bond USG adjust (mA)	−10	−5	0	5	10	Avg
Ball diameter (μm)	33.7	33.7	33.8	34	33.9	33.8
Ball height (μm)	8.4	8.8	7.8	8	8.1	8.2
Al splash (μm)	36.4	37.6	38.4	38	38.5	37.8
Shear force (N)	0.081	0.090	0.096	0.106	0.112	0.097
Shear/area (μN/μm ²)	91.23	100.36	107.96	117.08	124.69	107.96
Avg pull strength (N)	0.060	0.061	0.063	0.063	0.063	0.062
Min pull strength (N)	0.056	0.043	0.059	0.060	0.059	0.055
Peeling rate (%)	0	0	0	0	0	0

Table A.4 First bond USG experimental results for PdCu wire [51]

Bond USG adjust (mA)	−10	−5	0	5	10	Avg
Ball diameter (μm)	32.5	32.9	32.8	32.9	33.2	32.8
Ball height (μm)	8.4	7.7	8.1	8	7	7.8
Al splash (μm)	37.2	37.4	37.8	37.6	37.9	37.6
Shear force (N)	0.082	0.092	0.103	0.105	0.113	0.099
Shear/area (μN/μm ²)	98.84	109.48	121.64	124.69	129.25	117.08
Avg pull strength (N)	0.069	0.070	0.071	0.071	0.072	0.071
Min pull strength (N)	0.066	0.066	0.069	0.067	0.071	0.068
Peeling rate (%)	0	0	0	0	0	0

Table A.5 First bond force experimental results for Cu wire [51]

Bond force adjust (mA)	−7	−3.5	0	3.5	7	Avg
Ball diameter (μm)	33.6	34	33.8	34	34.5	34
Ball height (μm)	8.5	8.4	8.6	8.5	8	8.4
Al splash (μm)	37.3	37.7	37.3	38	38.3	37.7
Shear force (N)	0.098	0.100	0.103	0.106	0.108	0.103
Shear/area (μN/μm ²)	111.00	111.00	115.56	115.56	115.56	114.04
Avg pull strength (N)	0.064	0.067	0.066	0.065	0.065	0.065
Min pull strength (N)	0.053	0.063	0.063	0.061	0.061	0.060
Peeling rate (%)	0	0	0	0	0	0

Table A.6 First bond force experimental results for PdCu wire [51]

Bond force adjust (mA)	−7	−3.5	0	3.5	7	Avg
Ball diameter (μm)	32.4	32.4	33	32.9	33	32.7
Ball height (μm)	7.8	8	7.9	7.6	7.6	7.8
Al splash (μm)	36.7	38.1	38.0	38.0	38.3	37.8
Shear force (N)	0.097	0.100	0.103	0.107	0.108	0.103
Shear/area (μN/μm ²)	117.08	121.64	121.64	126.21	126.21	121.64
Avg pull strength (N)	0.072	0.072	0.069	0.068	0.071	0.070
Min pull strength (N)	0.069	0.069	0.060	0.062	0.068	0.066
Peeling rate (%)	0	0	0	0	0	0

Table A.7 Bake test results for PdCu and Cu wire bonds [51]

DOE Cell	Wire	24-hour Bake Test			168-hour Bake Test		
		Peel %	Avg pull strength (N)	Min pull strength (N)	Peel %	Avg pull strength (N)	Min pull strength (N)
USG adjust -10	PdCu	80	0.053	0.035	95	0.043	0.029
	Cu	0	0.063	0.060	50	0.052	0.020
USG adjust -5	PdCu	35	0.065	0.028	95	0.044	0.034
	Cu	0	0.062	0.060	25	0.059	0.042
USG adjust 0	PdCu	15	0.072	0.051	80	0.052	0.030
	Cu	0	0.062	0.060	40	0.059	0.040
USG adjust +5	PdCu	5	0.073	0.064	75	0.051	0.020
	Cu	0	0.063	0.061	10	0.062	0.055
USG adjust +10	PdCu	40	0.065	0.035	65	0.056	0.032
	Cu	5	0.062	0.043	5	0.062	0.045
Force adjust -7	PdCu	50	0.063	0.038	75	0.047	0.027
	Cu	0	0.064	0.060	5	0.063	0.041
Force adjust -3.5	PdCu	30	0.068	0.042	80	0.050	0.025
	Cu	0	0.061	0.056	10	0.066	0.061
Force adjust 0	PdCu	35	0.065	0.039	80	0.052	0.029
	Cu	0	0.063	0.060	5	0.063	0.060
Force adjust 3.5	PdCu	30	0.069	0.045	80	0.057	0.037
	Cu	0	0.063	0.060	0	0.064	0.059
Force adjust 7	PdCu	30	0.068	0.041	75	0.064	0.039
	Cu	0	0.063	0.060	5	0.064	0.056

Table A.8 Second bond USG DOE results for Cu wire [51]

USG (mA)	70	80	90	100	110	Avg
Avg stitch pull strength (N)	0.037	0.041	0.038	0.035	0.033	0.037
Min stitch pull strength (N)	0.029	0.036	0.029	0.003	0.003	0.020
Avg tail pull strength (N)	0.006	0.005	0.007	0.007	0.006	0.006
Min tail pull strength (N)	0.004	0.004	0.005	0.005	0.005	0.004

Table A.9 Second bond USG DOE results for PdCu wire [51]

USG (mA)	70	80	90	100	110	Avg
Avg stitch pull strength (N)	0.034	0.036	0.038	0.034	0.036	0.036
Min stitch pull strength (N)	0.024	0.026	0.016	0.013	0.023	0.021
Avg tail pull strength (N)	0.008	0.008	0.009	0.01	0.01	0.009
Min tail pull strength (N)	0.006	0.005	0.006	0.007	0.007	0.006

Table A.10 Second bond force DOE results for Cu wire [51]

USG (mA)	65	75	85	95	105	Avg
Avg stitch pull strength (N)	0.042	0.039	0.036	0.036	0.036	0.038
Min stitch pull strength (N)	0.036	0.030	0.030	0.026	0.027	0.029
Avg tail pull strength (N)	0.006	0.006	0.005	0.005	0.007	0.006
Min tail pull strength (N)	0.004	0.005	0.004	0.001	0.005	0.004

Table A.11 Second bond force DOE results for PdCu wire [51]

USG (mA)	65	75	85	95	105	Avg
Avg stitch pull strength (N)	0.035	0.034	0.034	0.038	0.036	0.036
Min stitch pull strength (N)	0.021	0.013	0.021	0.030	0.014	0.020
Avg tail pull strength (N)	0.009	0.009	0.008	0.010	0.010	0.009
Min tail pull strength (N)	0.007	0.007	0.006	0.008	0.007	0.007

Table A.12 Bare copper wire—reliability risk matrix

Environmental stress	Failure mechanism	Failure modes	Root cause	Test metric “detection”
Dry belt furnace or box oven 150 °C/min 4 h depending on moisture loss studies of the package	<ul style="list-style-type: none">Moisture-driven mechanismsWetting problems	<ul style="list-style-type: none">Broken bondsPackage mechanical damageDelaminationNot wet condition during bonding	<ul style="list-style-type: none">Hygroscopic/thermal stressesOxidation of CuAdhesion concerns with molding compound	<ul style="list-style-type: none">Open circuit/electrical testSonoscan for delamination check
<i>Preconditioning</i> MSL3: 260 °C, 3× reflow	<ul style="list-style-type: none">Moisture-drivenPopcorningDelamination	Broken bonds	Hygroscopic/thermal stresses	<ul style="list-style-type: none">Open circuit/electrical testSonoscan for delamination check
<i>Post preconditioning</i> Thermal cycling: (–55 to 125 °C) 1,000 cycles uHAST: 120 °C/85 % RH, 96 h	Thermal fatigue <ul style="list-style-type: none">ElectromigrationElectrical parametric shifts	Broken bonds	Thermomechanical stresses	Open circuit/electrical test
PCT: 120 °C/100 % RH, 96 h THB: 5 V @ 85 °C/85 % RH, 1,000 h BHAST: 5 V @ 120 °C/85 % RH, 96 h High temperature storage @ 175 °C, 1,000 h	Electromigration <ul style="list-style-type: none">Microstructural degradationExcessive IMC formationElectrical parametric shifts	Bond degradation Bond-to-bond metal migration Bond-to-bond metal migration Bond degradation	Bond corrosion Ionic transfer Ionic transfer <ul style="list-style-type: none">OxidationIMC evolution	Open circuit/electrical test Short circuit/electrical test Short circuit/electrical test Open circuit/electrical test
HTOL: 1 A, 1,000 h @ 150 °C	Electromigration and electrical parametric shift	Bond voids	IMC metal migration	Open circuit/electrical test
Thermal shock: (–55 to 125 °C) 100 cycles	Thermal fatigue	Broken bonds	Thermomechanical stresses	Open circuit/electrical test

Table A.13 Palladium-coated copper wire—reliability risk matrix

Environmental stress	Failure mechanism	Failure modes	Root cause	Test metric “detection”
Dry belt furnace or box oven 150 °C: min 4 h depending on moisture loss studies of the package	Moisture-driven mechanisms	<ul style="list-style-type: none">• Broken bonds• Package mechanical damage• Delamination	Hygroscopic/thermal stresses	<ul style="list-style-type: none">• Open circuit/electrical test• Sonoscan for delamination check
<i>Preconditioning</i> MSL3: 260 °C, 3 × reflow	<ul style="list-style-type: none">• Moisture-driven• Popcorning• Delamination	Broken bonds	Hygroscopic/thermal stresses	<ul style="list-style-type: none">• Open circuit/electrical test• Sonoscan for delamination check
<i>Post preconditioning</i> Thermal cycling: (–55 to 125 °C) 1,000 cycles	Thermal fatigue	Broken bonds	Thermo-mechanical stresses	Open circuit/electrical test
UHASt: 120 °C/85 % RH, 96 h	<ul style="list-style-type: none">• Electromigration• Electrical parametric shifts	Bond degradation	Bond corrosion	Open circuit/electrical test
PCT: 120 °C/100 % RH, 96 h	Electromigration	Bond degradation	Bond corrosion	Open circuit/electrical test
THB: 5 V @ 85 °C/85 % RH, 1,000 h	Electromigration	Bond-to-bond metal migration	Ionic transfer	Short circuit/electrical test
BHAST: 5 V @ 120 °C/85 % RH, 96 h	Electromigration	Bond-to-bond metal migration	Ionic transfer	Short circuit/electrical test
High-temperature storage: 175 °C, 1,000 h	<ul style="list-style-type: none">• Microstructural degradation• Excessive IMC formation• Electrical parametric shifts	Bond degradation	Oxidation, IMC evolution	Open circuit/electrical test
HTOL: 1 A, 1,000 h @ 150 °C	<ul style="list-style-type: none">• Electromigration• Electrical parametric shift	Bond voids	IMC metal migration	Open circuit/electrical test
Thermal shock: (–55 °C, 125 °C) 100 cycles	Thermal fatigue	Broken bonds	Thermo-mechanical stresses	Open circuit/electrical test

Appendix B: Patents on Copper Wire Bonding

The patents on Cu wire bonding can be broadly divided into the areas of bonding wire and fabrication, structure, ultrasonic methods, cover gas, capillary, and specialized applications such as reverse bonding, photovoltaic cell, optoelectronics, QFN, and power electronics. The patents on copper wire bonding from 1983 to 2012 are listed below.

1. Bonding wire for semiconductor

United States Patent 20120118610

May 17, 2012

Inventor: Shinichi Terashima, Tomohiro Uno, Takashi Yamada, Daizo Oda

Assignees: Nippon Micrometal Corporation, Nippon Steel Materials Co., Ltd.

Abstract: There is provided a bonding wire for semiconductors, capable of ensuring favorable wedge bondability even when bonded to a palladium-plated lead frame, superior in oxidation resistivity, and having a core wire of copper or a copper alloy. This bonding wire comprises: a core wire of copper or a copper alloy; a coating layer containing palladium and having a thickness of 10–200 nm; and an alloy layer formed on a surface of the coating layer, such alloy layer containing a noble metal and palladium and having a thickness of 1–80 nm. The aforementioned noble metal is either silver or metal, and a concentration of such noble metal in the alloy layer is not less than 10 % and not more than 75 % by volume.

2. Brace for long wire bond

United States Patent 20120145446

Jun 14, 2012

Inventor: Jie Yang, Qingchin He, Hanmin Zhang

Assignees: Freescale Semiconductor, Inc.

Abstract: An electrical connection includes a first wire bonded to adjacent bond pads proximate to an edge of a die and a second wire having one end bonded to a die bond pad distal to the die edge and a second end bonded to a lead finger of a lead frame or a connection pad of a substrate. The second wire crosses and is supported by the first wire. The first wire acts as a brace that prevents the second wire from

touching the edge of the die. The first wire also prevents the second wire from excessive lateral movement during encapsulation.

3. Copper bonding compatible bond pad structure and method

United States Patent 20120064711

Mar 15, 2012

Inventor: Francois Hebert, Anup Bhalla

Abstract: A copper bonding compatible bond pad structure and associated method is disclosed. The device bond pad structure includes a buffering structure formed of regions of interconnect metal and regions of non-conductive passivation material, the buffering structure providing buffering of underlying layers and structures of the device.

4. Copper bonding method

United States Patent 8148256

Apr 3, 2012

Inventor: Francois Hebert, Anup Bhalla

Assignee: Alpha and Omega Semiconductor Incorporated

Abstract: A copper bonding compatible bond pad structure and associated method is disclosed. The device bond pad structure includes a buffering structure formed of regions of interconnect metal and regions of non-conductive passivation material, the buffering structure providing buffering of underlying layers and structures of the device.

5. Method of making a copper wire bond package

United States Patent 20120164794

Jun 28, 2012

Inventor: Yan Xun Xue, Jun Lu, Anup Bhalla

Abstract: A method for making a wire bond package, comprising the step of providing a lead frame array comprising a plurality of lead frame units therein, each lead frame unit comprises a first die pad and a second die pad each having a plurality of tie bars connected to the lead frame array, a plurality of reinforced bars interconnecting the first and second die pads; the reinforced bars are removed after molding compound encapsulation.

6. Method of thermosonic wire bonding process for copper connection in a chip

United States Patent 6886735

May 3, 2005

Inventor: Jeng; Yeau-Ren, Wang; Chang-Ming

Assignee: National Chung Cheng University

Abstract: The present invention provides a method of thermosonic wire bonding process for a copper interconnected chip. It generates a copper oxide film in the range from 0.805 to 0.82 μm . By the barrier function of the copper oxide film, the bonding characteristic is improved.

7. Methods of forming wire bonds for wire loops and conductive bumps

United States Patent 20120074206

Mar 29, 2012

Inventor: Wei Qin, Jon W. Brunner, Paul A. Reid

Assignee: Kulicke and Soffa Industries, Inc.

Abstract: A method of forming a wire bond using a wire bonding machine is provided. The method includes the steps of: (1) selecting at least one target bonding control value; (2) generating bonding parameters for forming a wire bond using an algorithm and the at least one selected target bonding control value; (3) forming a wire bond using the generated bonding parameters; (4) determining if the at least one selected target bonding control value of the formed wire bond is within a predetermined tolerance of the at least one selected target bonding control value; (5) adjusting at least one bonding adjustment value if the at least one selected target bonding control value of the formed wire bond is not within the predetermined tolerance; and (6) generating revised bonding parameters for forming a subsequent wire bond using an algorithm and the at least one adjusted bonding adjustment value

8. Wire bonding

United States Patent EP0276564 A1, US4976393, Aug 3, 1988; Dec 11, 1990;
EP0276564 B1 Mar 11, 1992

Inventor: Isao Araki, Hitachikaminakaishataku Toshio, No. D-101 Chuma, Kazuo Hatori, Masahiro Koizumi, Makoto Nakajima, Yosho Ohashi, Susumu Okikawa, Jin Onuki, Hitoshi Suzuki

Assignee: Hitachi, Ltd.

Abstract: In ball bonding, a ball is formed on the end of a wire by an electric discharge between the wire and a discharge electrode. The ball is subsequently pressed onto a pad of a semiconductor pellet and bonded thereto by press bonding under heat with the application of ultrasonic vibrations. However, the pressing of the ball onto the pad may damage the pellet if the ball is too hard. Therefore, a reducing gas is supplied to the environs of the ball during its formation, the gas being supplied at a temperature preferably between 100 and 200 °C. This shows the cooling of the ball resulting in a finer crystal structure, and a lower hardness. Hence the occurrence of cracking of the pellet is reduced.

9. Fine copper wire for electronic instruments and method of manufacturing the same

United States Patent EP0296596 A1

Dec 28, 1988

Inventor: Yasuji Fujii, Toshiaki Inaba, Masaaki Kurihara, and Toru Tanigawa

Assignee: Furukawa Special Metal Co., Ltd, Furukawa Electric Co., Ltd.

Abstract: A fine copper wire for electronic instruments is disclosed which comprises 0.05–10 ppm in total amount of either one or not less than two kinds of Ti, Zr, V, Hf, Cr, Ca, Mg, Y and rare-earth elements, 1–30 ppm of oxygen and the remainder of Cu. A method of manufacturing therefore is described wherein the hot rolling is given to the ingot obtained by melting and casting in a non-oxidative atmosphere or in a vacuum, then stretch processing and at least one or more times of

intermediate annealing are repeated to finish to a fixed diameter of wire, and thereafter annealing is carried out under non-oxidative or reducible atmosphere to obtain desired mechanical characteristics.

10. Wire bonding process

United States Patent EP1139413 A2, EP1139413 B1 Oct 4, 2001; Mar 16, 2005

Inventor: Gonzalo Amador, Willmar E. Subido, Howard R. Test

Assignee: Texas Instruments Incorporated

Abstract: A robust, reliable and low-cost metal structure and process enabling electrical wire/ribbon connections to the interconnecting copper metallization of integrated circuits. The structure comprises a layer of barrier metal that resists copper diffusion, deposited on the non-oxidized copper surface in a thickness such that the barrier layer reduces the diffusion of copper at 250 °C by more than 80 % compared with the absence of the barrier metal. The structure further comprises an outermost bondable layer which reduces the diffusion of the barrier metal at 250 °C by more than 80 % compared with the absence of the bondable metal. Finally, a metal wire is bonded to the outermost layer for metallurgical connection. The barrier metal is selected from a group consisting of nickel, cobalt, chromium, molybdenum, titanium, tungsten, and alloys thereof. The outermost bondable metal layer is selected from a group consisting of gold, platinum, and silver.

11. Bonding wire for semiconductor devices

United States Patent EP2200076 A1

Jun 23, 2010

Inventor: Keiichi Kimura, Tomohiro Uno, Takashi Yamada

Assignee: Nippon Micrometal Corporation, Nippon Steel Materials Co., Ltd.

Abstract: It is an object of the present invention to provide a highly-functional bonding wire which has good wire-surface nature, loop linearity, stability of loop heights, and stability of a wire bonding shape, and which can cope with semiconductor packaging technologies, such as thinning, achievement of a fine pitch, achievement of a long span, and three-dimensional packaging. A semiconductor-device bonding wire comprises a core member formed of an electrically-conductive metal, and a skin layer mainly composed of a face-centered cubic metal different from the core member and formed thereon. The percentage of orientations in crystalline orientations in the lengthwise direction in the surface of the skin layer is greater than or equal to 50 %.

12. Bonding wire for semiconductor device

United States Patent EP2239766 A1

Oct 13, 2010

Inventor: Keiichi Kimura, Tomohiro Uno, Takashi Yamada

Assignee: Nippon Micrometal Corporation, Nippon Steel Materials Co., Ltd.

Abstract: An object of the present invention is to provide a high-performance bonding wire that is suitable for semiconductor mounting technology, such as stacked chip bonding, thinning, and fine pitch mounting, where wire lean (leaning) at an upright position of a ball and spring failure can be suppressed and loop linearity and loop height stability are excellent. This bonding wire for a semiconductor device includes a core material made of a conductive metal, and a

skin layer formed on the core material and containing a metal different from the core material as a main component; wherein a relationship between an average size (a) of crystal grains in the skin layer on a wire surface along a wire circumferential direction and an average size (b) of crystal grains in the core material on a normal cross section, the normal cross section being a cross section normal to a wire axis, satisfies an inequality of $a/b \leq 0.7$.

13. Semiconductor device bonding wire and wire bonding method

United States Patent EP2221861 A1

Aug 25, 2010

Inventor: Keiichi Kimura, Akihito Nishibayashi, Shinichi Terashima, Tomohiro Uno, Takashi Yamada

Assignee: Nippon Micrometal Corporation, Nippon Steel Materials Co., Ltd.

Abstract: It is an object of the present invention to provide a copper-based bonding wire whose material cost is low, having excellent ball bondability, reliability in a heat cycle test or reflow test, and storage life, enabling an application to thinning of a wire used for fine pitch connection. The bonding wire includes a core material having copper as a main component and an outer layer which is provided on the core material and contains a metal M and copper, in which the metal M differs from the core material in one or both of components and composition. The outer layer is 0.021–0.12 μm in thickness.

14. Method of and device for wire bonding with onsite gas generator

United States Patent EP2308632 A1

Apr 13, 2011

Inventor: Pang Ling Hiew, Christoph Laumen

Assignee: Linde Aktiengesellschaft

Abstract: The present invention relates to a device for wire bonding comprising a guidance for a bond wire and a melt inducing device for melting the surface of a definite region of the bond wire surface, whereby the bond wire guidance is adapted to guide the definite region of the bond wire into a bonding area and connect it to at least one bond pad, whereby the bonding area comprises a process gas inlet, wherein the process gas inlet is connected to an on-site gas generator which generates the process gas. In addition, the present invention relates to a method of wire bonding comprising the steps of: connecting a definite region of a guided bond wire to a bond pad, whereby the surface of the definite region is previously melted and the whole process takes place within a bonding area, which contains a process gas, which is led into the bonding area prior or during the bonding process, wherein at least a part of the process gas is generated by an on-site gas generator.

15. Semiconductor device bonding wire

United States Patent EP2312628 A2

Apr 20, 2011

Inventor: Keiichi Kimura, Akihito Nishibayashi, Shinichi Terashima, Tomohiro Uno, Takashi Yamada

Assignee: Nippon Micrometal Corporation, Nippon Steel Materials Co., Ltd.

Abstract: It is an object of the present invention to provide a copper-based bonding wire whose material cost is low, having excellent ball bondability, reliability in a heat cycle test or reflow test, and storage life, enabling an application to thinning of

a wire used for fine pitch connection. The bonding wire includes a core material having copper as a main component and an outer layer which is provided on the core material and contains a metal M and copper, in which the metal M differs from the core material in one or both of components and composition. The outer layer is 0.021–0.12 μm in thickness.

16. Semiconductor device with copper wire ball bonding

United States Patent 5023697

Jun 11, 1991

Inventor: Kiyoaki Tsumura

Assignee: Mitsubishi Denki Kabushiki Kaisha

Abstract: A semiconductor device in accordance with the present invention includes a semiconductor chip which is bonded to a die pad using a solder having a liquidus temperature of 370 °C or less. A copper ball is moved to contact an Al electrode pad on the semiconductor chip in less than 150 ms after formation of the ball. Plastic deformation takes place so that the copper ball is pressed against the aluminum electrode pad and the height of the copper ball becomes 25 μm or less. It is possible to firmly wire the Al pad on the semiconductor chip and the inner lead frame without cracking the glass coating by utilizing a silver plating on the die pad and an Au-metallized layer on the rear side of the semiconductor chip. It is also possible to decrease the work hardening property of the Cu ball and prevent Al exudation when the Cu ball is bonded to the Al electrode pad.

17. Capillary for bonding copper wires between a semiconductor circuit chip and a corresponding terminal connector of a semiconductor device

United States Patent 6581816

Jun 24, 2003

Inventor: Battista Vitali, Alessandro Frontero

Assignee: STMicroelectronics S.r.l.

Abstract: A capillary for electrical bonding between a semiconductor chip and corresponding pins of a semiconductor device in which the chip is accommodated includes a body whose terminal portion is substantially frustum-shaped. The body has a diametrical through hole which allows the passage of a copper wire for electrical bonding between the chip and the semiconductor device. The portion of the body that is adjacent a lower end of the through hole is flared, with a flaring diameter and a flaring angle which allows formation of a substantially flat annular peripheral region on a copper ball when the copper ball is placed at a lower end of the copper wire. The copper ball is deformed by the action of the capillary. The formation of the substantially flat annular peripheral region is independent of the position of the copper wire within the through hole of the body of the capillary.

18. Copper alloy bonding wire for semiconductor device

United States Patent 8004094

Aug 23, 2011

Inventor: Tomohiro Uno, Keiichi Kimura, Takashi Yamada**Assignee:** Nippon Steel Materials Co., Ltd., Nippon Micrometal Corporation

Abstract: The present invention provides a semiconductor-device copper-alloy bonding wire which has an inexpensive material cost, ensures a superior ball joining shape, wire joining characteristic, and the like, and a good loop formation characteristic, and a superior mass productivity. The semiconductor-device copper-alloy bonding wire contains at least one of Mg and P in total of 10–700 mass ppm, and oxygen within a range from 6 to 30 mass ppm.

19. Wire bonding structure and method for forming same

United States Patent US8247911 B2

Aug 21, 2012

Inventor: Keiichi Kimura, Akihito Nishibayashi, Shinichi Terashima, Tomohiro Uno, Takashi Yamada**Assignee:** Nippon Micrometal Corporation, Nippon Steel Materials Co., Ltd.

Abstract: Provided is a bonding structure of a bonding wire and a method for forming the same which can solve problems of conventional technologies in practical application of a multilayer copper wire, improve the formability and bonding characteristic of a ball portion, improve the bonding strength of a wedge connection, and have a superior industrial productivity. A bonding wire mainly composed of copper, and a concentrated layer where the concentration of a conductive metal other than copper is high is formed at a ball bonded portion. The concentrated layer is formed in the vicinity of the ball bonded portion or at the interface thereof. An area where the concentration of the conductive metal is 0.05–20 mol % has a thickness greater than or equal to 0.1 μm , and it is preferable that the concentration of the conductive metal in the concentrated layer should be five times as much as the average concentration of the conductive metal at the ball bonded portion other than the concentrated layer.

20. Copper on organic solderability preservative (OSP) interconnect and enhanced wire bonding process

United States Patent US8247272 B2

Aug 21, 2012

Inventor: Ronaldo Cayetano Calderon, Kian Teng Eng, Yong Chuan Koh, Rodel Manalac, Pang Hup Ong, Jr. Lope Vallespin Pepito, Jeffrey Nantes Salamat, Jimmy Siat**Assignee:** United Test and Assembly Center Ltd.

Abstract: A semiconductor package and a method for constructing the package are disclosed. The package includes a substrate and a die attached thereto. A first contact region is disposed on the substrate and a second contact region is disposed on the die. The first contact region, for example, comprises copper coated with an OSP material. A copper wire bond electrically couples the first and second contact regions. Wire bonding includes forming a ball bump on the first contact region having a flat

top surface. Providing the flat top surface is achieved with a smoothing process. A ball bond is formed on the second contact region, followed by stitching the wire onto the flat top surface of the ball bump on the first contact region.

21. Ultrasonic transducers for wire bonding and methods of forming wire bonds using ultrasonic transducers

United States Patent US8251275 B2

Aug 28, 2012

Inventor: Dominick A. DeAngelis, Gary W. Schulze

Assignee: Kulicke and Soffa Industries, Inc.

Abstract: A method of forming a wire bond using a bonding tool coupled to a transducer is provided. The method includes the steps of: (1) applying electrical energy to a driver of the transducer at a first frequency; and (2) applying electrical energy to the driver at a second frequency concurrently with the application of the electrical energy at the first frequency, the first frequency and the second frequency being different from one another.

22. Wire bonding structure and method that eliminates special wire bondable finish and reduces bonding pitch on substrates

United States Patent US8269356 B2

Sep 18, 2012

Inventor: Byung Joon Han, Hun Teak Lee, and Rajendra D. Pendse

Assignee: Stats Chippac Ltd.

Abstract: A semiconductor package has a semiconductor die disposed on a substrate. A bond wire is connected between a first bonding site on the semiconductor die and a second bonding site on the substrate. The first bonding site is a die bond pad; the second bonding site is a stitch bond. The second bonding site has a bond finger formed on the substrate, a conductive layer in direct physical contact with the bond finger, and a bond stud coupled to the bond wire and in direct physical contact with the conductive layer to conduct an electrical signal from the semiconductor die to the bond finger. The bond finger is made of copper. The conductive layer is made of copper or gold. The bond stud is made of gold and overlies a side portion and top portion of the copper layer.

23. Method of making a copper wire bond package

United States Patent US8283212 B2

Oct 9, 2012

Inventor: Anup Bhalla, Jun Lu, Yan Xun Xue

Assignee: Alpha & Omega Semiconductor, Inc.

Abstract: A method for making a wire bond package comprising the step of providing a lead frame array comprising a plurality of lead frame units therein, each lead frame unit comprises a first die pad and a second die pad each having a plurality of tie bars connected to the lead frame array, a plurality of reinforced bars interconnecting the first and second die pads; the reinforced bars are removed after molding compound encapsulation.

24. Copper pad for copper wire bonding

United States Patent US 20100052174 A1

Mar 4, 2010

Inventor: Mark Bachman, John Osenbach**Assignee:** Agere Systems Inc.

Abstract: An integrated circuit package comprising an integrated circuit that includes transistors coupled to copper interconnect structures. The integrated circuit package also comprises copper pads located on the integrated circuit and directly contacting uppermost ones of the copper interconnect structures. Each of the copper pads has a thickness of at least about 2 μm . The integrated circuit package further comprises copper wires pressure welded directly to the copper pads.

25. Semiconductor device and method for producing the same

United States Patent US 2011/0304046 A1

Dec 15, 2011

Inventor: Takashi Kitazawa, Yasushige Sakamoto, Motoaki Wakui**Assignee:** On Semiconductor Trading, Ltd., a Bermuda Limited Company,

Abstract: A semiconductor element is secured to an island, and a plurality of through-holes are formed in the portion of the island, which surrounds the area to which the semiconductor element is secured. Further, the electrode pads of the semiconductor element and leads are electrically connected by copper wires. In this structure, the cost of materials is reduced by using the copper wires in comparison with gold wires. Further, a part of a resin package is embedded in through-holes, so that the island can be easily supported within the resin package.

26. Epoxy resin composition for semiconductor encapsulation, cured product thereof, and semiconductor device

United States Patent US20120261807 A1

Oct 18, 2012

Inventor: Shingo Itoh, Shinichi Zenbutsu

Abstract: An epoxy resin composition for semiconductor encapsulation of the present invention contains an epoxy resin and a curing agent and is used to encapsulate a copper wire and a semiconductor element connected to this copper wire. This epoxy resin composition is such that when a cured product of the epoxy resin composition is heated for 10 hours at 200 °C, the amount of generation of a first corrosive gas that is a sulfur compound having corrosiveness to the copper wire is less than or equal to 70 ppm.

27. Semiconductor device bonding wire and wire bonding method

United States Patent 8102061

Jan 24, 2012

Inventor: Tomohiro Uno, Keiichi Kimura, Shinichi Terashima, Takashi Yamada, Akihito Nishibayashi

Abstract: It is an object of the present invention to provide a copper based bonding wire whose material cost is low, having excellent ball bondability, reliability in a heat cycle test or reflow test, and storage life, enabling an application to thinning of a wire used for fine pitch connection. The bonding wire includes a core material having copper as a main component and an outer layer which is provided on the

core material and contains a metal M and copper, in which the metal M differs from the core material in one or both of components and composition. The outer layer is 0.021–0.12 μm in thickness.

28. Semiconductor package using copper wires and wire bonding method for the same

United States Patent 20080265385

Oct 30, 2010

Inventor: HanLung Tsai, ChihMing Huang, ChengHsu Hsiao

Assignee: Siliconware Precision Industries Co., Ltd

Abstract: A semiconductor package using copper wires and a wire bonding method for the same are proposed. The package includes a carrier having fingers and a chip mounted on the carrier. The method includes implanting stud bumps on the fingers of the carrier and electrically connecting the chip and the carrier by copper wires with one end of the copper wires being bonded to bond pads of the chip and the other end of the copper wires being bonded to the stud bumps on the carrier. The implanted stud bumps on the carrier improve bondability of the copper wires to the carrier and thus prevent stitch lift. With good bonding, residues of copper wires left behind after a bonding process have even tail ends and uniform tail length to enable fabrication of solder balls of uniform size, thereby eliminating a conventional step of implanting stud bumps on the bond pads of chips and preventing ball lift from occurring.

29. Ultrasonic wire bonding method for a semiconductor device

United States Patent 20120164795

Jun 28, 2012

Inventor: Masahiko Sekihara, Takanori Okita

Assignee: Renesas Electronics Corporation

Abstract: A risk of an electrical short between electrode pads of a semiconductor device can be reduced to thereby improve quality of the semiconductor device. During ball bonding in wire bonding, in each of the electrode pads of a semiconductor chip which are arrayed along an ultrasonic wave application direction (ultrasonic vibration direction), a ball at the tip of a copper wire and the electrode pad are coupled to each other while being rubbed against each other in a direction intersecting the ultrasonic wave application direction. Thus, the amount of Al splash formed on the electrode pad can be minimized to make the Al splash smaller. As a result, the quality of the semiconductor device assembled by the above mentioned ball bonding can be improved.

30. Semiconductor device with copper wire ball bonding

United States Patent 5023697

Jun 1, 1991

Inventor: Tsumura Kiyoaki

Assignee: Mitsubishi Denki Kabushiki Kaisha

Abstract: A semiconductor device in accordance with the present invention includes a semiconductor chip which is bonded to a die pad using a solder having a liquidus temperature of 370 °C or less. A copper ball is moved to contact an Al electrode pad on the semiconductor chip in less than 150 ms after formation of the ball. Plastic deformation takes place so that the copper ball is pressed against the

aluminum electrode pad and the height of the copper ball becomes 25 μm or less. It is possible to firmly wire the Al pad on the semiconductor chip and the inner lead frame without cracking the glass coating by utilizing a silver plating on the die pad and an Au metallized layer on the rear side of the semiconductor chip. It is also possible to decrease the work hardening property of the Cu ball and prevent Al exudation when the Cu ball is bonded to the Al electrode pad.

31. Wire bonding over active circuits

United States Patent 20090236742

Sep 24, 2009

Inventor: Qwai H. Low

Assignee: LSI Corporation

Abstract: A semiconductor device includes a semiconductor die mounted over a package substrate. The die has a bond pad located thereover. A stud bump consisting substantially of a first metal is located on the bond pad. A wire consisting substantially of a different second metal is bonded to the stud bump.

32. Wire bonding structure and manufacturing method thereof

United States Patent US7859123

Dec 28, 2010

Inventor: Chung Hsing Tzu

Assignee: Great Team Backend Foundry, Inc.

Abstract: The present invention relates to a wire bonding structure, and more particularly to a manufacturing method for said wire bonding structure. The wire bonding structure comprises a die that connects with a lead via a bonding wire. At least one bond pad is positioned on an active surface of the die, and a gold bump is provided on the bond pad; furthermore, a ball bond can be positioned upon the gold bump. The bond pad and the gold bump can separate the ball bond and the die, which can avoid damaging the die during the bonding process.

33. Wirebonding method and device enabling high speed reverse wedge bonding of wire bonds

United States Patent 20120032354

Feb 9, 2012

Inventor: Ken Pham, Luu T. Nguyen

Assignee: National Semiconductor Corporation

Abstract: Methods and systems are described for enabling the efficient fabrication of wedge bonding of integrated circuit systems and electronic systems. In particular, a reverse bonding approach can be employed.

34. Wirebonding process

United States Patent 20110192885

Aug 11, 2011

Inventor: Hendrik Pieter Hochstenbach, Willem Dirk Van Driel, Eric Ooms

Assignee: NXP B.V.

Abstract: Consistent with an example embodiment, a wirebonding process comprises forming a bond pad with a roughened upper surface, lowering a copper wirebond ball onto the roughened bond pad, and applying a force to the wirebond ball against the roughened surface. A heat treatment is applied to form the bond between the wirebond ball and the roughened surface, wherein the bond is formed without use of ultrasonic energy. This process avoids the use of ultrasonic

welding and thereby reduces the occurrence of microcracks and resulting chip out of the bond (COUB) and metal peel off (MPO) failures. The roughened surface of the bond pad improves the reliability of the connection.

35. Wire bonding technique for integrated circuit chips

United States Patent EP0073172 A2

Mar 2, 1983

Inventor: Donald E. Cousens, John A. Kurtz

Assignee: Fairchild Camera & Instrument Corporation

Abstract: In a method for welding a lead wire or bonding wire from a microcircuit chip mounted on a lead frame to a lead frame finger, the lead frame finger is preheated prior to any substantial electrical or thermal coupling between the lead frame finger and chip. Intense but controlled energy is applied to the lead frame finger at levels which might otherwise damage the IC chip. In one embodiment, the lead frame finger is preheated to a temperature below the melting point of the metal comprising the lead frame. Enhanced bonding is thereafter affected by thermocompression bonding or the like. In another embodiment, the preheating step comprises melting a portion of the surface of the lead frame finger and forming a molten pool or puddle in the surface. Bonding of the lead wire is affected by immersing a section of the wire in the molten pool or puddle. In order to preheat the lead frame finger a controlled pulse train is delivered for arc discharge at the bonding location. Bonding apparatus and circuitry for performing the method are described.

36. Semiconductor device comprising an electrode pad

United States Patent EP0271110 A2, Jun 15, 1988; Feb 22, 1989; Oct 6, 1993
EP0271110 A3, EP0271110 B1

Inventor: Osamu C/O Patent Division Usuda

Assignee: Kabushiki Kaisha Toshiba

Abstract: In a semiconductor device in which copper or copper alloy bonding wire is bonded to an electrode pad on a semiconductor element, the electrode pad is formed of a first metal layer ohmically contacting the semiconductor element, a second metal layer hard enough not to be deformed at wire bonding step, and a third metal layer for bonding a copper wire, to suppress variation in the electric characteristics of a bonding portion and the production of strain in the semiconductor element at wire bonding step.

37. Ultrasonic wire bonding method

United States Patent EP0286031 A2

Oct 12, 1988

Inventor: Shigeo Hara, Kazunori Hori, Tokiyuki Seto, Minoru Taguchi

Assignee: Hitachi Computer Peripherals Co., Ltd. and Hitachi, Ltd.

Abstract: The ultrasonic wire bonding method for bonding the conductor of a sheathed wire to the terminal of an electronic part comprises the steps of forming a first rough-finished surface on either a portion of the sheath of the sheathed wire or the end of a bonding tip which is to be in contact with the sheath and to impart an ultrasonic vibration to sheath, while forming a second rough-finished surface on either another portion of the sheath of the sheathed wire or the face of the terminal of the electronic part to which the conductor of the sheathed wire is to be bonded;

and placing the sheathed wire between the bonding tip and the terminal and imparting an ultrasonic vibration to the sheathed wire while lightly forcing the bonding tip to the terminal. The sheathed wire has the sheath thereof scraped without slipping and thus the conductor thereof naked, and this conductor is thereafter or simultaneously bonded to the terminal positively, which can improve the efficiency of wire bonding.

38. Method of soldering a copper wire to a silver contact on a silicon photovoltaic cell and application of said method to a plurality of silicon photovoltaic cells

United States Patent EP0503015 B1

Jul 11, 2001

Inventor: T. Jeffrey Borenstein, C. Ronald Gonsiorawski, J. Michael Kardauskas

Assignee: ASE Americas, Inc.

Abstract: Photovoltaic cells with silver-rich thick film electrical contacts and superior thermal aging properties are disclosed. Electrical wires are bonded to the silver rich thick film contacts using a tin and silver solder paste comprising between about 96 % tin/4 % silver and 98 % tin/2 % silver. Solar cells having soldered connections incorporating the present invention exhibit the capability of withstanding temperatures in the range of 150 °C with little or no deterioration of the solder bonds for periods far longer than conventionally prepared cells.

39. Cu-pad bonded to Cu-wire with self-passivating Cu-alloys

United States Patent EP1348235 A2

Oct 1, 2003

Inventor: Hans-Joachim Barth

Assignee: Infineon Technologies North America Corp.

Abstract: In an integrated circuit structure, the improvement comprising a wire bonded Cu pad with Cu-wire component, wherein the Cu-pad Cu-wire component is characterized by self-passivation, low resistance, high bond strength, and improved resistance to oxidation and corrosion, the Cu-pad Cu-wire component comprising: a metallization-line; a liner separating the metallization line and a Cu alloy surrounding a Cu-pad; a dielectric surrounding the liner; and a Cu-pad bonded to a Cu-alloy wire; the Cu-wire component being characterized by self-passivation areas on: (a) a dopant rich interface in between the Cu-alloy and liner; (b) a surface of the Cu-pad; (c) a surface of the bond between the Cu-pad and the Cu-alloy wire; and (d) a surface of the Cu-alloy wire.

40. Pre-cleaning of copper surfaces during Cu/Cu or Cu/Metal bonding using hydrogen plasma

United States Patent EP1353365 A2

Oct 15, 2003

Inventor: Yakub Aliyu, Simon Chooi, Subhash Gupta, Paul Kwok Keung Ho, Sudipto Ranendra Roy, John Leonard Sudijono, Yi Xu, Mei Sheng Zhou

Assignee: Chartered Semiconductor Manufacturing Pte Ltd.

Abstract: A method of bonding a wire to a metal bonding pad, comprising the following steps. A semiconductor die structure having an exposed metal bonding pad within a chamber is provided. The bonding pad has an upper surface. A hydrogen-plasma is produced within the chamber from a plasma source. The

metal bonding pad is pre-cleaned and passivated with the hydrogen-plasma to remove any metal oxide formed on the metal bonding pad upper surface. A wire is then bonded to the passivated metal bonding pad.

41. Method of removing oxide from copper bond pads

United States Patent EP1388167 A2

Feb 11, 2004

Inventor: Bte Fuaida Harun, Bin Faizairi Mohd Mohd Nor, Wai Kok Mui, Chu Lan Tan

Assignee: Motorola, Inc.

Abstract: A method of preparing a semiconductor wafer having integrated circuits formed on it that have pads formed of copper includes the steps of removing oxide from the copper pads and then vacuum packing the wafer in a shock-proof container. The oxide may be removed from the copper pads in a number of ways. A first way includes cleaning the wafer in an alkaline solution, performing acid neutralization on the cleaned wafer, and then drying the wafer. A second way includes cleaning the wafer with an acid solution, rinsing the acid cleaned wafer with water, applying an anti-oxidant activator to the surface of the copper pads, rinsing the wafer with water after the application of the anti-oxidant activator, and then drying the water rinsed wafer. Yet a third way includes plasma cleaning the copper pads using a combination of about 5–10 % Hydrogen and about 90–95 % Argon and then sputtering a very thin layer of aluminum on a surface of the copper pads. The layer of aluminum has a thickness of about 1–5 nm.

42. Method of removing oxide from copper bond pads

United States Patent EP1388167 B1

Aug 23, 2006

Inventor: Bte Fuaida Harun, Bin Faizairi Mohd Mohd Nor, Wai Kok Mui, Chu Lan Tan

Assignee: Freescale Semiconductor, Inc.

Abstract: A method of preparing a semiconductor wafer having integrated circuits formed on it that have pads formed of copper includes the steps of removing oxide from the copper pads and then vacuum packing the wafer in a shock-proof container. The oxide may be removed from the copper pads in a number of ways. A first way includes cleaning the wafer in an alkaline solution, performing acid neutralization on the cleaned wafer, and then drying the wafer. A second way includes cleaning the wafer with an acid solution, rinsing the acid cleaned wafer with water, applying an anti-oxidant activator to the surface of the copper pads, rinsing the wafer with water after the application of the anti-oxidant activator, and then drying the water rinsed wafer. Yet a third way includes plasma cleaning the copper pads using a combination of about 5–10 % Hydrogen and about 90–95 % Argon and then sputtering a very thin layer of aluminum on a surface of the copper pads. The layer of aluminum has a thickness of about 1–5 nm.

43. Bonding wire

United States Patent EP1447842 A1

Aug 18, 2004

Inventor: Inc. M. Sumitomo Electric Wintec Fukagaya, Inc. M. Sumitomo Electric Wintec Ioka, S. Sumitomo Electric Ind. Ltd. Kaimori, Inc. T. Sumitomo Electric Wintec Nonaka

Assignee: Sumitomo Electric Wintec, Incorporate

Abstract: A bonding wire having a core mainly consisting of copper and a coating layer formed on the core, wherein the coating layer is made of an oxidation-resistant metal having a melting point higher than that of copper, and the elongation of this bonding wire per unit sectional area is $0.021\text{ \%}/\text{m}^2$ or more; and a bonding wire having a core mainly consisting of copper and a coating layer formed on the core, wherein the coating layer is made of a metal having oxidation resistance higher than that of copper, and the relationship of $0.007 \leq X \leq 0.05$ is satisfied wherein an area ratio X is (the area of the coating layer/the area of the core at the section of wire being cut vertically) are provided. The bonding wires thus provided are inexpensive and excellent in ball formation characteristic and bonding characteristic. Further, a ball bonding method characterized using the above bonding wire is also provided.

44. Bonding wire and integrated circuit device using the same

United States Patent EP1677345 A1

Jul 5, 2005

Inventor: Inc. Sumitomo Electric Wintec Masanori Ioka, Osaka Works Sumitomo Elect. Ind. Ltd. S. Kaimori, Inc. Sumitomo Electric Wintec Tsuyoshi Nonaka

Assignee: Sumitomo Electric Industries Ltd.

Abstract: A bonding wire comprising a core and a coating layer formed on the core, wherein the coating layer is formed from a metal having a higher melting point than the core, and further has at least one of the following characteristics: (1) the wet contact angle with the coating layer when the core is melted is not smaller than 20° ; (2) when the bonding wire is hung down with its end touching a horizontal surface, and is cut at a point 15 cm above the end and thus let drop onto the horizontal surface, the curvature radius of the formed arc is 35 mm or larger; (3) the 0.2 % yield strength is not smaller than $0.115\text{ mN}/\mu\text{m}^2$ but not greater than $0.165\text{ mN}/\mu\text{m}^2$; or (4) the Vickers hardness of the coating layer is 300 or lower.

45. Copper bonding or superfine wire with improved bonding and corrosion properties

United States Patent EP1856736 A1

Nov 21, 2007

Inventor: Albrecht Bischoff, Heinz Förderer, Frank Krüger, Lutz Schröpfer

Assignee: W.C. Heraeus GmbH

Abstract: The invention relates to a bonding or superfine wire made from copper, with a gold enrichment on the surface thereof, in particular to an amount corresponding to a coating of at most 50 nm, or which may be bonded by the

ball/wedge method, has a copper-colored appearance and the ball thereof after flame-off has a hardness of 95 by HV0.002. In order to produce said bonding or superfine wire, a copper wire is coated with gold or a copper-gold alloy or gold is introduced into the surface of the copper wire. Said wires are bonded to a semiconductor silicon chip.

46. Ultrahigh-purity copper and process for producing the same, and bonding wire comprising ultrahigh-purity copper

United States Patent EP1903119 A1

Mar 26, 2008

Inventor: Yuichiro Nippon Mining & Metals Co. Ltd., Shindo and Kouichi from Nippon Mining & Metals Co. Ltd., Takemoto

Assignee: JX Nippon Mining & Metals Co., Ltd.

Abstract: Provided is ultrahigh purity copper having a hardness of 40 Hv or less, and a purity of 8 N or higher (provided that this excludes the gas components of O, C, N, H, S and P). With this ultrahigh purity copper, the respective elements of O, S and P as gas components are 1wtppm or less. Also provided is a manufacturing method of ultrahigh purity copper based on two-step electrolysis using an electrolytic solution comprised of copper nitrate solution, including the procedures of adding hydrochloric acid in an electrolytic solution comprised of copper nitrate solution; circulating the electrolytic solution; and performing two-step electrolysis while eliminating impurities with a filter upon temporarily setting the circulating electrolytic solution to a temperature of 10 °C or less. The present invention provides a copper material that is compatible with the thinning (wire drawing) of the above, and is capable of efficiently manufacturing ultrahigh purity copper having a purity of 8 N (99.999999 wt%) or higher, providing the obtained ultrahigh purity copper, and providing a bonding wire for use in a semiconductor element that can be thinned.

47. Wire bonding capillary apparatus and method

United States Patent EP1904264 B1

Aug 10, 2011

Inventor: Alfred Steven Kummerl, P. Bernhard Lange

Assignee: Texas Instruments Inc.

Abstract: An apparatus and method for bonding a wire, such as a flat rectangular cross sectioned ribbon wire, to a work piece in semiconductor device fabrication. The wire is fed through a passageway of an ultrasonic bond capillary and clamped against an engagement surface of the bond capillary via a clamping jaw operably coupled to the bond capillary. The wire is bonded to the work piece along a bonding surface of the bond capillary and penetrated, at least partially, between the bonding surface and the engagement surface of the bond capillary by a cutting tool. The cutting tool may comprise an elongate member positioned between the bonding surface and engagement surface, and may have a cutting blade positioned at a distal end thereof. The cutting tool may further comprise a ring cutter, wherein the ribbon wire passes through a ring having a cutting surface defined about an inner diameter thereof.

48. Semiconductor device and method for fabricating semiconductor device

United States Patent US7936070

May 3, 2011

Inventor: Yumi Hayashi, Noriaki Matsunaga, Takamasa Usui**Assignee:** Kabushiki Kaisha Toshiba

Abstract: A semiconductor device includes: a copper (Cu) wire having a first region and a second region in which densities of silicon (Si) and oxygen (O) atoms are higher than in the first region; a compound film that is selectively formed on the Cu wire and contains Cu and Si; and a dielectric film formed on a side surface side of the Cu wire.

49. Optoelectronic device

United States Patent US20090127579

May 21, 2009

Inventor: Qinghuan Sun

Abstract: An optoelectronic device includes a base, first and second stands mounted on the base, a chip mounted on the first stand, a copper wire for bonding the chip to the second stand, and a molding compound mounted on the base. The molding compound encapsulates the first and the second stands, the chip, and the copper wire. The molding compound is made of epoxy resin.

50. Quad flat no-lead (QFN) chip package assembly apparatus and method

United States Patent US7402459

Jul 22, 2008

Inventor: Tan Xiaochun, Li Yunfang**Assignee:** Shanghai Kaihong Technology Co., Ltd

Abstract: In one embodiment, the present invention includes a method of fabricating a quad flat no-lead (QFN) chip package. The method includes forming a stamped lead frame; forming a die pad and a lead shrink on one side of the stamped lead frame; mounting a die on the die pad; performing wire bonding; encapsulating the die and the wire bond with a molding compound; removing the stamped lead frame after encapsulating; and sawing the molding compound after the stamped lead frame has been removed. Such method results in improved quality of wire leads, improved lifespan of cutting blades, and reduction of burrs as compared to many existing methods of fabricating QFN chip packages.

51. Method of fabricating a wire bond pad with Ni/Au metallization

United States Patent US7294565

Jul 22, 2008

Inventors: Lloyd G. Burrell, Charles R. Davis, Ronald D. Goldblatt, William F. Landers, Sanjay C. Mehta**Assignee:** International Business Machines Corporation

Abstract: A method for sealing an exposed surface of a wire bond pad with a material that is capable of preventing a possible chemical attack during electroless deposition of Ni/Au pad metallurgy is provided. Specifically, the present invention provides a method whereby a TiN/Ti or TiN/Al cap is used as a protective coating covering exposed surfaces of a wire bond pad. The TiN/Ti or TiN/Al cap is not affected by alkaline chemistries used in forming the Ni/Au metallization, yet it provides a sufficient electrical pathway connecting the bond pads to the Ni/Au pad metallization.

52. Semiconductor device with a copper wires ball bonded to aluminum electrodes

United States Patent US5229646

Jul 20, 1993

Inventor: Kiyoaki Tsumura**Original Assignee:** Mitsubishi Denki Kabushiki Kaisha

Abstract: A semiconductor device formed by a semiconductor chip bonded to a lead frame die pad. The bonding material, such as a silicone resin, has an elasticity modulus ranging from 1 to 100 kg/cm² from room temperature to 400 °C. The lead frame electrodes are connected to the semiconductor chip electrodes by copper alloy wires.

53. Corrosion-resistant copper-to-aluminum bonds

United States Patent US20120001336

Jan 5, 2012

Inventors: Kejun Zeng, Wei Qun Peng**Original Assignee:** Texas Instruments Incorporated

Abstract: A connection formed by a copper wire alloyed with a noble metal in a first concentration bonded to a terminal pad of a semiconductor chip; the end of the wire being covered with a zone including an alloy of copper and the noble metal in a second concentration higher than the first concentration. When the noble metal is gold, the first concentration may range from about 0.5–2.0 wt%, and the second concentration from about 1.0–5.0 wt%. The zone of the alloy of the second concentration may have a thickness from about 20 to 50 nm.

54. Resin packaged semiconductor device having a protective layer made of a metal-organic matter compound

United States Patent US4821148

Apr 11, 1989

Inventors: Shiro Kobayashi, Masahiko Itoh, Akira Minato**Original Assignee:** Hitachi, Ltd.

Abstract: A silver electrode on a lead frame is bonded to an aluminum electrode on a silicon chip with a copper wire. The resulting semiconductor device was immersed in a solution of benzotriazole in ethyl alcohol. An Ag-benzotriazole film was formed on the surface of the silver electrode and a Cu-benzotriazole film was formed on the surface of the copper wire, while an Al-benzotriazole film was formed on the surface of the aluminum electrode. Even if water penetrates into the semiconductor device, the silver electrode, the aluminum electrode and the copper wire are effectively protected by the anti-corrosive Ag-benzotriazole film, Cu-benzotriazole film and Al-benzotriazole film to exhibit excellent damp-proof.

55. Active solid-state devices (e.g., transistors, solid-state diodes) lead frame with structure for mounting semiconductor chip to lead frame (e.g., configuration of die bonding flag, absence of a die bonding flag, recess for lead)

United States Patent US4821148

Jul 12, 2012

Inventors: Shinichi Zenbutsu (Shinagawa-Ku, JP)

Abstract: Disclosed is a semiconductor device consisting of a lead frame or a circuit board, at least one semiconductor element which is stacked on or mounted in parallel on the lead frame or on the circuit board, a copper wire which electrically

connects the lead frame or the circuit board to the semiconductor element, and an encapsulating material which encapsulates the semiconductor element and the copper wire, wherein the wire diameter of the copper wire is equal to or more than 18 μm and equal to or less than 23 μm , the encapsulating material is composed of a cured product of an epoxy resin composition, the epoxy resin composition contains an epoxy resin, a curing agent, a spherical silica, and a metal hydroxide and/or metal hydroxide solid solution, and the semiconductor device is obtained through a step of encapsulating by the epoxy resin composition and molding, and then segmenting the resultant into pieces.

56. Wire bonding insulated wire

United States Patent US6854637

Jul 20, 1993

Inventors: Fuaida Harun, Kong Bee Tiu**Original Assignee:** Freescale Semiconductor, Inc.

Abstract: An electrical connection for connecting a bond pad of a first device and a bond pad of a second device with an insulated or coated wire. The electrical connection includes a first wire bond securing a first portion of the insulated bond wire to the first device bond pad. A second wire bond secures a second portion of the insulated bond wire to the second device bond pad. A bump is formed over the second wire bond, and the bump is offset from the second wire bond. The offset bump enhances the second bond, providing it with increased wire peel strength.

57. Method of manufacturing semiconductor device, and wire bonder

United States Patent 20100203681

Aug 12, 2010

Inventors: Kazuyuki Misumi, Hideyuki Arakawa, Shunji Yamauchi, Mitsuru Aoki**Original Assignee:** Renesas Technology Corp.

Abstract: An improvement in the quality of wire bonding is achieved by reducing the vibration of a lead frame or a wiring substrate after wire bonding. Over a heat block in a wire bond portion of a wire bonder, there is provided a cooling blower for cooling a wire-bonded matrix frame so that the temperature thereof may decrease stepwise. After wire bonding, cold air is blown from the cooling blower to the matrix frame, and temperature control of the matrix frame is performed so that the temperature of the matrix frame after wire bonding may decrease stepwise. Or, the wire-bonded matrix frame is fixed with a holding tool such as a frame holding member, a guide member, a roller means, or an elastic means until cooling is completed.

58. Two step wire bond process

United States Patent US6461898

Oct 8, 2002

Inventors: Seok Mo Kwon, Si Hyun Choe**Original Assignee:** Motorola, Inc.

Abstract: A two-step wire bonding process is used to ultrasonically attach a wire to a contact pad on a semiconductor device. A first step is used to flatten a rounded tip of the wire, and to start the bonding process. This is accomplished by applying a relatively large force to the rounded tip, and a relatively low vibrating displacement

to the flattened wire tip. During a second step, the large force is reduced, however; the vibrating displacement is increased. The total time for the two step wire bonding process is slightly less than a prior art one step process.

59. Copper interconnect for an integrated circuit and methods for its fabrication

United States Patent US6373137

Apr 16, 2002

Inventor: Allen McTeer

Original Assignee: Micron Technology, Inc.

Abstract: A multi layered copper bond pad for a semiconductor die which inhibits formation of copper oxide is disclosed. A small dose of titanium is implanted in the copper surface. The implanted titanium layer suppresses the copper oxide growth in the copper bond pad by controlling the concentration of vacancies available to the copper ion transport. An interconnect structure such as a wire bond or a solder ball may be attached to the copper–boron layer to connect the semiconductor die to a lead frame or circuit support structure. In another embodiment, a titanium–aluminum passivation layer for copper surfaces is also disclosed. The titanium–aluminum layer is annealed to form a titanium–aluminum–copper alloy. The anneal may be done in a nitrogen environment to form a titanium–aluminum–copper–nitrogen alloy.

60. Manufacturing method for resin sealed semiconductor device

United States Patent US7271035

Sep 18, 2007

Inventor: Noriyuki Kimura

Original Assignee: Seiko Instruments Inc.

Abstract: A semiconductor device manufacturing method comprises etching a front side of a conductive board to form plural sets of a die pad portion and bonding areas, each set corresponding to one semiconductor device. Semiconductor chips are mounted on respective ones of the die pad portions using conductive paste. Electrodes of the respective semiconductor chips are electrically connected with metal wires to the bonding areas, and then the front side of the conductive board, including the semiconductor chips, the bonding areas and the metal wires, are sealed with a molding resin to form a resin-sealed body. Thereafter, the whole back side of the conductive board is removed to a depth sufficient to expose the die pad portions and the bonding areas. Then the resin-sealed body is separated into individual semiconductor devices.

61. Electrode structure of a semiconductor device which uses a copper wire as a bonding wire

United States Patent US5293073

Mar 8, 1994

Inventor: Tadaaki Ono

Original Assignee: Kabushiki Kaisha Toshiba

Abstract: A semiconductor device comprises a semiconductor substrate, a first insulation film formed on the semiconductor substrate, a metal film for forming a

bonding pad on the first insulation film, and a second insulation film which is formed between the first insulation film and the bonding pad and which is stiffer than the first insulation film.

62. Power composite integrated semiconductor device and manufacturing method thereof

United States Patent US7416932

Aug 26, 2008

Inventor: Hiroyasu Itou

Original Assignee: Denso Corporation

Abstract: A high-reliability power composite integrated semiconductor device uses thick copper electrodes as current collecting electrodes of a power device portion to resist wire resistance needed for reducing ON-resistance. Furthermore, wire bonding connection of the copper electrodes is secured, and also the time-lapse degradation under high temperature, which causes diffusion of copper and corrosion of copper, is suppressed. Furthermore, a direct bonding connection can be established to current collecting electrodes in the power device portion, and also established to a bonding pad formed on the control circuit portion in the control circuit portion. A pad area at the device peripheral portion which has been hitherto needed is reduced, so that the area of the device is saved, and the manufacturing cost is reduced.

63. Method of producing semiconductor device

United States Patent US5116783

May 26, 1992

Inventor: Kiyooki Tsumura

Original Assignee: Mitsubishi Denki Kabushiki Kaisha

Abstract: A method of producing a semiconductor device includes bonding a semiconductor chip to a die pad of a lead frame by means of a silicone resin, to bonding a copper wire and an aluminum electrode of the semiconductor chip in such a manner that intermetallic compound mainly consisting of CuAl_2 is formed in the bonding region. This method suppresses the deterioration of the copper–aluminum alloy layer and these semiconductor devices have a high reliability at a high temperature, as well as uniform quality in the production.

64. Semiconductor device including an electrode

United States Patent US5298793

Mar 29, 1994

Inventors: Jutaro Kotani, Masahiro Ihara, Hideaki Nakura, Masami Yokozawa

Original Assignee: Matsushita Electronics Corporation

Abstract: There is disclosed a semiconductor device having an electrode for wire bonding, comprising a first aluminum layer, a nickel–aluminum alloy layer, and a second aluminum layer. The electrode is suitable for bonding with copper wire, since the electrode withstands a wide range of bonding conditions—mechanical pressure, ultrasonic wave power and such, and permits a reliable electrical connection to be maintained.

65. Anti-oxidation system of a wire bonder using a copper wire

United States Patent US4995552

Feb 26, 1991

Inventors: Wan-Kyoon Choi, Jong-Whan Kim**Original Assignee:** Samsung Electronics Co. Ltd.

Abstract: An anti-oxidation system of a wire bonder for bonding a wire between a chip pad and a lead frame for a semiconductor device, said wire being comprised of an oxidizable material such as copper or aluminum, wherein a reduction gas for preventing oxidation of the wire is periodically supplied around a spool wound by said wire, at least one gas tube for supplying the reduction gas is disposed towards both sides of a capillary device drawing out the wire, said gas tubes being disposed just beneath the end of capillary device in opposite directions to each other, and a torch being disposed facing with a lower surface of either one of said gas tubes and just beneath the capillary device.

66. Semiconductor electronic device and method of manufacturing thereof

United States Patent US20040072396

May 29, 2003

Inventors: Roberto Tiziani, Loic Renard, Battista Vitali**Original Assignee:** STMicroelectronics S.r.l.

Abstract: A semiconductor electronic device is disclosed, which includes a die of a semiconductor material and a holder connected electrically together by wire leads of copper, the semiconductor material die being formed with a plurality of contact pads; the device being characterized by having a welding stud bump of a metal material selected from a group comprising gold, palladium, and alloys thereof, formed on each contact pad in said plurality, each copper wire lead being welded with one end on a stud bump and with the other end to said holder. This electronic device is highly reliable and can be fabricated simply at a low cost.

67. Pressure sense die pad layout and method for direct wire bonding to programmable compensation integrated circuit die

United States Patent US7677109

Mar 16, 2010

Inventors: Ian Bentley, Alistair D. Bradley**Original Assignee:** Honeywell International Inc.

Abstract: A method for direct die-to-die wire bonding incorporates a pressure sense die and a programmable compensation IC die that can be mounted on a ceramic substrate. The two die can be positioned beside each other such that wire bond pads on the pressure sense die and bonding leads on the compensation IC die are in same order. The pressure sense die and the compensation IC can be connected directly with wire bonds in order to reduce the number of wire bonds and to improve reliability. The pressure sense die can be designed with multiple wire bond pad patterns in order to be utilized with different programmable compensation IC dies.

68. Semiconductor device using bonding wires of different materials

United States Patent US5173762

Dec 22, 1992

Inventor: Masaki Ota**Original Assignee:** Kabushiki Kaisha Toshiba

Abstract: Disclosed is a semiconductor device comprising a semiconductor integrated chip having at least a power processing circuit in which a larger current flows and a signal processing circuit in which a smaller current flows, each circuit having bonding pads, a package having lead frames, on which the semiconductor integrated chip is mounted, and a plurality of bonding wires with different materials through which the bonding pads are joined to the lead frames.

69. Roughened bonding pad and bonding wire surfaces for low pressure wire bonding

United States Patent US7015580

Mar 21, 2006

Inventors: John A. Fitzsimmons, Jeffrey P. Gambino, Erick G. Walton

Original Assignee: International Business Machines Corporation

Abstract: An intermediate semiconductor structure and method for low-pressure wire bonding that reduces the propensity of dielectric material to mechanical failure due to any wire bonding stresses. Roughened surfaces such as metal pillars or metal dendrites are provided on a bonding pad, bonding wire or both. These roughened surfaces increase reactivity between the bond wire and the bond pad to form strong bonds. This increased activity as a result of the roughened bonding pad and/or wire surfaces reduce the amount of pressure, temperature and energy required for wire bonding, which in turn, avoids damage to the bonding pad as well as the semiconductor substrate.

70. Method of producing a wire bonding ball

United States Patent US4739142

Apr 19, 1988

Inventors: Jitsuho Hirota, Kazumichi Machida, Masaaki Shimotomai

Original Assignee: Mitsubishi Denki Kabushiki Kaisha

Abstract: A method of producing a wire bonding ball for ball bonding a metal wire to an electrode of a semiconductor chip involves producing a ball by melting the top end of the metal wire by a discharge which is conducted by applying a high voltage between said metal wire and a discharge electrode in an inactive gas ambient. The metal wire is at a positive voltage said the discharge electrode is at a negative voltage, respectively. Next, a later period of discharge is conducted by inverting the voltage polarities of the discharge electrode elements. The metal wire used is a material capable of being oxidated.

71. Semiconductor device

United States Patent US20110074019

Mar 31, 2011

Inventors: Masatoshi Yasunaga, Hironori Matsushima, Kenya Hironaga, Soshi Kuroda

Abstract: To improve the reliability of a semiconductor device in which wire bonding using a wire made of copper is performed. A semiconductor device is configured so that one of end parts (wide width part) of a copper wire is joined via a bump on a pad (electrode pad) formed over a main surface (first main surface) of a semiconductor chip of the semiconductor device. The bump is made of gold, which is a metal material having a hardness lower than that of copper, and the width of the bump is narrower than the width of the wide width part of the wire.

72. Semiconductor package having oxidation-free copper wire

United States Patent US20030173659

Sep 18, 2003

Inventors: Sang-do Lee, Yong-suk Kwon, Jong-jin Shin**Original Assignee:** Fairchild Korea Semiconductor Ltd.

Abstract: A semiconductor package having an oxidation free copper wire that connects a semiconductor chip and a pad is provided. The copper wire is coated with an oxidation free layer. The copper wire provides good electrical characteristics and reliability.

73. Manufacturing method for resin sealed semiconductor device

United States Patent US7550322

Jun 23, 2009

Inventor: Noriyuki Kimura**Original Assignee:** Seiko Instruments Inc.

Abstract: A semiconductor device manufacturing method comprises etching a front side of a conductive board to form plural sets of a die pad portion and bonding areas, each set corresponding to one semiconductor device. Semiconductor chips are mounted on respective ones of the die pad portions using conductive paste. Electrodes of the respective semiconductor chips are electrically connected with metal wires to the bonding areas, and then the front side of the conductive board, including the semiconductor chips, the bonding areas and the metal wires, are sealed with a molding resin to form a resin-sealed body. Thereafter, the back side of the conductive board is selectively removed, such as by etching, to leave the die pad portions and the bonding areas protruding from a bottom surface of the resin-sealed body. Then, the resin-sealed body is separated into individual semiconductor devices.

74. Gas delivery system for reducing oxidation in wire bonding operations

United States Patent US8066170

Nov 29, 2011

Inventors: Gary S. Gillotti, Stanley Szczesniak, Peter J. Van Emmerik**Original Assignee:** Kulicke and Soffa Industries, Inc.

Abstract: A wire bonding machine is provided. The wire bonding machine includes a bonding tool and an electrode for forming a free air ball on an end of a wire extending through the bonding tool where the free air ball is formed at a free air ball formation area of the wire bonding machine. The wire bonding machine also includes a bond site area for holding a semiconductor device during a wire bonding operation. The wire bonding machine also includes a gas delivery mechanism configured to provide a cover gas to: (1) the bond site area whereby the cover gas is ejected through at least one aperture of the gas delivery mechanism to the bond site area, and (2) the free air ball formation area.

75. Ultrasonic wire bonding method for a semiconductor device

United States Patent US20120164795

Jun 28, 2012

Inventors: Masahiko Sekihara, Takanori Okita**Original Assignee:** Renesas Electronics Corporation

Abstract: A risk of an electrical short between electrode pads of a semiconductor device can be reduced to thereby improve quality of the semiconductor device.

During ball bonding in wire bonding, in each of the electrode pads of a semiconductor chip which are arrayed along an ultrasonic wave application direction (ultrasonic vibration direction), a ball at the tip of a copper wire and the electrode pad are coupled to each other while being rubbed against each other in a direction intersecting the ultrasonic wave application direction. Thus, the amount of Al splash formed on the electrode pad can be minimized to make the Al splash smaller. As a result, the quality of the semiconductor device assembled by the above-mentioned ball bonding can be improved.

76. Two step wire bond process

United States Patent US6165888

Dec 26, 2000

Inventors: Seok Mo Kwon, Si Hyun Choe**Original Assignee:** Motorola, Inc.

Abstract: A two-step wire bonding process is used to ultrasonically attach a wire to a contact pad on a semiconductor device. A first step is used to flatten a rounded tip of the wire, and to start the bonding process. This is accomplished by applying a relatively large force to the rounded tip, and a relatively low vibrating displacement to the flattened wire tip. During a second step, the large force is reduced, however; the vibrating displacement is increased. The total time for the two step wire bonding process is slightly less than a prior art one step process.

77. Aluminum and copper bimetallic bond pad scheme for copper damascene interconnects

United States Patent US6376353

Apr 23, 2002

Inventors: Mei Sheng Zhou, Sangki Hong, Simon Chooi**Original Assignee:** Chartered Semiconductor Manufacturing Ltd.

Abstract: Improved processes for fabricating wire bond pads on pure copper damascene are disclosed by this invention. The invention relates to various methods of fabrication used for semiconductor integrated circuit devices, and more specifically, to the formation of AlCu alloy top pad metal layers, which improve adhesion among the wire bond, top AlCu and the underlying copper pad metallurgy. This invention describes processes wherein a special AlCu bond layer or region is placed on top of the underlying copper pad metal. This AlCu bond pad on pure copper (with barrier layer in-between) provides for improved wire bond adhesion to the bond pad and prevents peeling during wire bond adhesion tests.

78. Wire for bonding a semiconductor device

United States Patent US4717436

Jan 5, 1988

Inventors: Naoyuki Hosoda, Masaki Morikawa, Naoki Uchiyama, Hideaki Yoshida, Toshiaki Ono**Original Assignee:** Mitsubishi Kinzoku Kabushiki Kaisha

Abstract: The present invention eliminates the problems associated with the use of oxygen-free copper and other high-purity copper materials as bonding wires. In accordance with one aspect of the present invention, at least one rare earth

element, or at least one element selected from the group consisting of Mg, Ca, Ti, Zr, Hf, Li, Na, K, Rb and Cs, or the combination of at least one rare earth element and at least one element selected from the above-specified group is incorporated in high-purity copper as a refining component in an amount of 0.1–100 ppm on a weight basis, and the high-purity copper is subsequently refined by zone melting. The very fine wire drawn from the so refined high-purity copper has the advantage that it can be employed in high-speed ball bonding of a semiconductor chip with a minimum chance of damaging the bonding pad on the chip by the ball forming at the tip of the wire.

79. Method of using hydrogen plasma to pre-clean copper surfaces during Cu/Cu or Cu/metal bonding

United States Patent US6720204

Jan 5, 1988

Inventors: John Leonard Sudijono, Yakub Aliyu, Mei Sheng Zhou, Simon Chooi, Subhash Gupta, Sudipto Ranendra Roy, Paul Kwok Keung Ho, Yi Xu

Original Assignee: Chartered Semiconductor Manufacturing Ltd.

Abstract: A method of bonding a wire to a metal bonding pad, comprising the following steps. A semiconductor die structure having an exposed metal bonding pad within a chamber is provided. The bonding pad has an upper surface. A hydrogen-plasma is produced within the chamber from a plasma source. The metal bonding pad is pre-cleaned and passivated with the hydrogen-plasma to remove any metal oxide formed on the metal bonding pad upper surface. A wire is then bonded to the passivated metal bonding pad.

80. Structure of electrode junction for semiconductor device

United States Patent US5003373

Mar 26, 1991

Inventors: Kiyooki Tsumura, Hitoshi Fujimoto

Original Assignee: Mitsubishi Denki Kabushiki Kaisha

Abstract: A structure of an electrode junction for a semiconductor device comprises an insulating film covering the entire surface of a silicon substrate, an aluminum electrode layer which is formed on the insulating film, a copper ball bonded on the electrode layer, and a copper-aluminum alloy layer continuously formed from the copper ball to the aluminum electrode layer. The aluminum layer under the copper ball is not separated from the aluminum layer surrounding the copper ball, so that alloy layer deterioration along the periphery thereof does not cause the electrical resistance to increase. This structure will increase the device life time to the maximum level.

81. Method of application of copper solution in flip-chip, COB, and micrometal bonding

United States Patent US6415973

Jul 9, 2002

Inventors: Kwok Keung Paul Ho, Simon Chooi, Yi Xu, Mei Sheng Zhou, Yakub Aliyu, John Leonard Sudijono, Subhash Gupta, Sudipto Ranendra Roy

Original Assignee: Chartered Semiconductor Manufacturing Ltd.

Abstract: A method of bonding a bonding element to a metal bonding pad, comprising the following steps. A semiconductor structure having an exposed

metal bonding pad within a passivation layer opening is provided. The bonding pad has an upper surface. A bonding element is positioned to contact the bonding pad upper surface. A bonding solution is applied within the passivation layer opening, covering the bonding pad and a portion of the bonding element. The structure is annealed by heating said bonding element to selectively solidify the bonding solution proximate said contact of said bonding element to said bonding pad, bonding the bonding element to the bonding pad.

82. Wire bonding over active circuits

United States Patent US8125091

Feb 28, 2012

Inventor: Qwai H. Low**Original Assignee:** LSI Corporation

Abstract: A semiconductor device includes a semiconductor die mounted over a package substrate. The die has a bond pad located thereover. A stud bump consisting substantially of a first metal is located on the bond pad. A wire consisting substantially of a different second metal is bonded to the stud bump.

83. Low cost bonding pad and method of fabricating same

United States Patent US7245025

Jul 17, 2007

Inventors: Jeffrey Alan Brigante, Zhong-Xiang He, Barbara Ann Waterhouse, Eric Jeffrey White**Original Assignee:** International Business Machines Corporation

Abstract: A structure and a method of forming the structure. The structure including: an integrated circuit chip having a set of wiring levels from a first wiring level to a last wiring level, each wiring level including one or more damascene, dual-damascene wires or damascene vias embedded in corresponding interlevel dielectric levels, a top surface of a last damascene or dual-damascene wire of the last wiring level substantially coplanar with a top surface of a corresponding last interlevel dielectric level; a capping layer in direct physical and electrical contact with a top surface of the last damascene or dual-damascene wire, the last damascene or dual-damascene wire comprising copper; a dielectric passivation layer formed on a top surface of the last interlevel dielectric level; and an aluminum pad in direct physical and electrical contact with the capping layer, a top surface of the aluminum pad not covered by the dielectric passivation layer.

84. Capillary for wire bonding

United States Patent US7427009

Sep 23, 2008

Inventors: Loon A Lim, Charles J Vath, III**Original Assignee:** ASM Technology Singapore Pte Ltd.

Abstract: A capillary tip for deforming a bonding wire during bonding of the wire to a bonding surface comprises a bottom face along an inner periphery of the capillary tip for pressing the bonding wire against a bonding surface, an outer radius along an outer periphery of the capillary tip, and includes a first inclined face adjacent to the bottom face and extending obliquely to the bottom face as well as a second inclined face adjacent to the first inclined face and extending obliquely to the first inclined face.

85. Copper on organic solderability preservative (OSP) interconnect and enhanced wire bonding process

United States Patent US20100025849

Feb 4, 2010

Inventors: Yong Chuan Koh, Jimmy Siat, Jeffrey Nantes Salamat, Lope Vallespin Pepito, Jr., Ronaldo Cayetano Calderon, Rodel Manalac, Pang Hup Ong, Kian Teng Eng

Original Assignee: United Test and Assembly Center Ltd.

Abstract: A semiconductor package and a method for constructing the package are disclosed. The package includes a substrate and a die attached thereto. A first contact region is disposed on the substrate and a second contact region is disposed on the die. The first contact region, for example, comprises copper coated with an OSP material. A copper wire bond electrically couples the first and second contact regions. Wire bonding includes forming a ball bump on the first contact region having a flat top surface. Providing the flat top surface is achieved with a smoothing process. A ball bond is formed on the second contact region, followed by stitching the wire onto the flat top surface of the ball bump on the first contact region.

86. Fabrication method of semiconductor

United States Patent US20030059721

Mar 27, 2003

Inventors: Wen-Lo Shieh, Ning Huang, Hui-Pin Chen, Hua-Wen Chiang, Chung-Ming Chang, Feng-Chang Tu, Fu-Yu Huang, Hsuan-Jui Chang, Chia-Chieh Hu, Wen-Long Leu

Abstract: A fabrication method of semiconductor packaging and the packaging element is disclosed. A layer of copper is formed on a thick heat-resistant tape and the surface of the copper layer is coated with a light sensitive photoresist. A light source passes through a pre-fabricated circuit negative being performed on the copper layer such that the photoresist is retained on the surface of the copper layer. An etching step is performed so as to obtain a copper wire with circuit diagram. After that, a wire bonding or a flip chip method is used to bind copper wire circuit with the chip. An appropriate packaging method is performed, a packaging element is obtained after the heat-resistant tape is removed.

87. Bonding structure of bonding wire and method for forming same

United States Patent US20100213619

Aug 26, 2010

Inventors: Tomohiro Uno, Shinichi Terashima, Keiichi Kimura, Takashi Yamada, Akihito Nishibayashi

Original Assignees: Nippon Steel Materials Co., Ltd., Nippon Micrometal Corporation

Abstract: Provided is a bonding structure of a bonding wire and a method for forming the same which can solve problems of conventional technologies in practical application of a multilayer copper wire, improve the formability and bonding characteristic of a ball portion, improve the bonding strength of wedge connection, and have a superior industrial productivity. A bonding wire mainly composed of copper, and a concentrated layer where the concentration of a conductive metal other than copper is high is formed at a ball bonded portion.

The concentrated layer is formed in the vicinity of the ball bonded portion or at the interface thereof. An area where the concentration of the conductive metal is 0.05–20 mol % has a thickness greater than or equal to 0.1 μm , and it is preferable that the concentration of the conductive metal in the concentrated layer should be five times as much as the average concentration of the conductive metal at the ball bonded portion other than the concentrated layer.

88. Wire for bonding a semiconductor device and process for producing the same

United States Patent US4676827

Jun 30, 1987

Inventors: Naoyuki Hosoda, Masaki Morikawa, Naoki Uchiyama, Hideaki Yoshida, Toshiaki Ono

Original Assignee: Mitsubishi Kinzoku Kabushiki Kaisha

Abstract: The present invention eliminates the problems associated with the use of oxygen-free copper and other high-purity copper materials as bonding wires. At least one rare earth element, or at least one element selected from the group consisting of Mg, Ca, Ti, Zr, Hf, Li, Na, K, Rb and Cs, or the combination of at least one rare earth element and at least one element selected from the above-specified group is incorporated in high-purity copper as a refining component in an amount of 0.1–100 ppm on a weight basis, and the high-purity copper is subsequently refined by zone melting. The very fine wire drawn from the so refined high-purity copper has the advantage that it can be employed in high-speed ball bonding of a semiconductor chip with a minimum chance of damaging the bonding pad on the chip by the ball forming at the tip of the wire.

89. Copper on organic solderability preservative (OSP) interconnect

United States Patent US20090008796

Jan 8, 2009

Inventors: Kian Teng Eng, Wolfgang Johannes Hetzel, Werner Josef Reiss, Florian Ammer, Yong Chuan Koh, Jimmy Siat

Original Assignee: United Test and Assembly Center Ltd.

Abstract: Provided is a semiconductor package, and a method for constructing the same, including a first substrate, a first semiconductor chip attached to the first substrate, and a first copper wire. At least one of the first substrate and the first semiconductor chip has an Organic Solderability Preservative (OSP) material coated on at least a portion of one surface, and the first copper wire is wire bonded through the OSP material to the first substrate and the first semiconductor chip.

90. Semiconductor device having improved electrode pad structure

United States Patent US5060051

Oct 22, 1991

Inventor: Osamu Usuda

Original Assignee: Kabushiki Kaisha Toshiba

Abstract: In a semiconductor device in which copper or copper alloy bonding wire is bonded to an electrode pad on a semiconductor element, the electrode pad is formed of a first metal layer ohmically contacting the semiconductor element, a second metal layer hard enough not to be deformed at wire bonding step, and a third

metal layer for bonding a copper wire, to suppress variation in the electric characteristics of a bonding portion and the production of stain in the semiconductor element at wire bonding step.

91. Wire bonding apparatus and method

United States Patent US5452841

Sep 26, 1995

Inventors: Sinji Sibata, Shuji Sakou, Akihiko Ogino

Original Assignee: Nippondenso Co., Ltd.

Abstract: A wire bonding apparatus and method which enable fully automatic wire bonding between a connecting electrode on a circuit board and an external lead terminal while saving space to prevent enlargement of the package size. The wire bonding method has the steps of welding one end of a ribbon shaped flat copper wire to the terminal (external lead terminal); welding the other end of the copper wire to the pad (connecting electrode) which is disposed at a level below the level of the terminal, while turning the intermediate portion of the copper wire on and around the cylindrical portion of the forming member which is disposed at a level above the terminal within the horizontal span between the pad and the terminal; and depressing the bent portion of the copper wire which has been bent by being turned around the cylindrical portion of the forming member down to a level below the level of the terminal so that the copper wire, within the vertical span between the pad and the terminal, is bent to form the first acute bend and then bent back to form the second acute bend and then extended to the pad.

92. Semiconductor device and method of manufacturing the same

United States Patent US8227341

Jul 24, 2012

Inventors: Satoshi Onai, Minoru Akaishi, Hiroshi Ishizeki, Yoshiaki Sano

Original Assignees: Semiconductor Components Industries, Llc, Sanyo Semiconductor Co., Ltd.

Abstract: An object is to prevent a failure, such as a wiring separation or a crack, in an insulating film under a copper wire, in a semiconductor device formed by wire-bonding the copper wire on a portion above the copper wiring. A semiconductor device according to the present invention includes a copper wiring formed above a semiconductor substrate, a plated layer formed so as to cover a top surface and side surfaces of the copper wiring, and a copper wire which is wire-bonded on the plated layer above the copper wiring.

93. Copper bonding or superfine wire with improved bonding and corrosion properties

United States Patent US7645522

Jan 12, 2010

Inventors: Albrecht Bischoff, Heinz Förderer, Lutz Schräpler, Frank Krüger

Original Assignee: W.C. Heraeus GmbH

Abstract: A bonding or superfine wire is provided made of copper, with a gold enrichment on the surface thereof, in particular in an amount corresponding to a coating of at most 50 nm. The wire may be bonded by the ball/wedge method, has a copper-colored appearance, and the ball thereof after flame-off has a hardness of less

than 95 according to HV0.002. In order to produce the bonding or superfine wire, a copper wire is coated with gold or a copper-gold alloy or gold is introduced into the surface of the copper wire. The wires are bonded to a semiconductor silicon chip.

94. Wire bonding method, semiconductor chip, and semiconductor package

United States Patent US7067413

Jun 27, 2006

Inventors: Jin-Ho Kim, In-Ku Kang, Sang-Yeop Lee

Original Assignee: Samsung Electronics Co., Ltd.

Abstract: A method of wire bonding, a semiconductor chip, and a semiconductor package provides stitch-stitch bonds of a wire on a bond pad of a chip as well as on a bond position of a substrate. A ball-stitch bump is formed on an end of the wire extending from a capillary or provided on the bond pad of the chip. A ball-stitch bump is formed on the bond pad of the chip by pressing down the ball of the wire on the bond pad. A ball-stitch stitch bond of the wire is formed on the ball-stitch bump by pressing down the wire on the ball-stitch bump. The capillary is moved from the bond pad to the bond position, while loosening the wire. A stitch bond of the wire is formed on the bond position by pressing down the wire on the bond position, and then separated from the wire within the capillary. The method of wire bonding, a semiconductor chip, and a semiconductor package can reduce or minimize a moving path of the capillary and provide more effective wire bonding.

95. Supplying a cover gas for wire ball bonding

United States Patent US6234376

May 22, 2001

Inventor: Rudolph M. Wicen

Original Assignee: Kulicke & Soffa Investments, Inc.

Abstract: Method and apparatus for supplying a protective cover gas during ball formation on a wire bonding machine to permit the use of wire formed from metals which may react with air, such as copper or aluminum.

96. Copper alloy bonding wire for semiconductor device

United States Patent US8004094

Aug 23, 2001

Inventors: Tomohiro Uno, Keiichi Kimura, Takashi Yamada

Original Assignees: Nippon Steel Materials Co., Ltd., Nippon Micrometal Corporation

Abstract: The present invention provides a semiconductor-device copper-alloy bonding wire which has an inexpensive material cost, ensures a superior ball joining shape, wire joining characteristic, and the like, and a good loop formation characteristic, and a superior mass productivity. The semiconductor-device copper-alloy bonding wire contains at least one of Mg and P in total of 10 to 700 mass ppm, and oxygen within a range from 6 to 30 mass ppm.

97. Trench MOSFET with trench source contact having copper wire bonding

United States Patent US20100127323

Nov 26, 2008

Inventors: Ming-Tao Chung, Fu-Yuan Hsieh

Original Assignee: Force Mos Technology Co. Ltd.

Abstract: A trench MOSFET with trench source contact structure having copper wire bonding is disclosed. By employing the proposed structure, die size can be shrunk into

30–70 % with high cell density, and the spreading resistance is significantly reduced without adding expensive thick metal layer as prior art. To further reduce fabricating cost, copper wire bonding is used with requirement of thick Al alloys.

98. Semiconductor package having oxidation-free copper wire

United States Patent 20030173659

Sep 18, 2003

Inventors: Sang-do Lee, Yong-suk Kwon, Jong-jin Shin

Original Assignee: Fairchild Korea Semiconductor Ltd.

Abstract: A semiconductor package having an oxidation free copper wire that connects a semiconductor chip and a pad is provided. The copper wire is coated with an oxidation free layer. The copper wire provides good electrical characteristics and reliability.

99. Semiconductor device with copper wire ball bonding

United States Patent US5023697

Jun 11, 1991

Inventor: Kiyoaki Tsumura

Original Assignee: Mitsubishi Denki Kabushiki Kaisha

Abstract: A semiconductor device in accordance with the present invention includes a semiconductor chip which is bonded to a die pad using a solder having a liquidus temperature of 370 °C or less. A copper ball is moved to contact an Al electrode pad on the semiconductor chip in less than 150 ms after formation of the ball. Plastic deformation takes place so that the copper ball is pressed against the aluminum electrode pad and the height of the copper ball becomes 25 µm or less. It is possible to firmly wire the Al pad on the semiconductor chip and the inner lead frame without cracking the glass coating by utilizing silver plating on the die pad and an Au-metallized layer on the rear side of the semiconductor chip. It is also possible to decrease the work hardening property of the Cu ball and prevent Al exudation when the Cu ball is bonded to the Al electrode pad.

100. Advanced copper interconnect system that is compatible with existing IC wire bonding technology

United States Patent US5785236

Jul 28, 1998

Inventors: Robin. W. Cheung, Ming-Ren Lin

Original Assignee: Advanced Micro Devices, Inc.

Abstract: A process is provided which enables electrical connection to be formed between gold and aluminum wires and copper interconnects. Conventional techniques for wire bonding are ineffective for bonding gold wires or aluminum wires to copper pads or copper interconnects. A process is provided to modify the copper pads so that conventional wire bonding techniques can be employed. In the process of the present invention, an aluminum pad is formed over the copper interconnects. The metal wire is then bonded to the aluminum pad using conventional wire bonding techniques. No new hardware and/or technology is required for the metal wire bonding. No new technology is required to integrate the process of the invention into existing IC fabrication processes.

101. Integrated circuit with bonding layer over active circuitry

United States Patent US6144100

Nov 7, 2000

Inventors: Chi-Cheong Shen, Donald C. Abbott, Walter Bucksch, Marco Corsi, Taylor Rice Efland, John P. Erdeljac, Louis Nicholas Hutter, Quang Mai, Konrad Wagensohner, Charles Edward Williams

Original Assignee: Texas Instruments Incorporated

Abstract: An integrated circuit device with a bonding surface directly over its active circuitry, and a method of making such integrated circuits. To make the bonding surface, a wafer is provided with vias to its metallization layer and then coated with a seed metal layer. A plating pattern is formed on the wafer, exposing portions of the seed metal layer and blocking the rest of the seed metal layer. These exposed portions are plated with successive metal layers, thereby forming a bonding surface having a number of layered stacks that fill the vias. The plating pattern and the nonplated portions of the seed metal layer are then removed.

102. Concave face wire bond capillary

United States Patent US6158647

Dec 12, 2000

Inventors: Gregory M. Chapman, Michael J. Bettinger, Jennifer A. Due

Original Assignee: Micron Technology, Inc.

Abstract: An improved wire bonding capillary used in the bonding of wires to the bond pads of a semiconductor device and the leads of a lead frame. The wire bonding capillary having a working tip having a working surface including a flat annular portion surrounding the wire feed aperture in the capillary and a concave surface extending there from to the intersection with the radius extending from the external tip diameter of the working tip.

103. Control of size and heat affected zone for fine pitch wire bonding

United States Patent US6180891

Jan 30, 2001

Inventor: Nikhil M. Murdeshwar

Original Assignee: International Business Machines Corporation

Abstract: The amount of melting of the bonding wire is closely regulated, and reduction of size and improvement of uniformity of the free air ball is obtained for ball bonding at pitches of less than ninety mils even when bonding wire of reduced diameter is employed. Quenching of the bonding wire adjacent to the free air ball also limits the temperature rise in the bonding wire and the extent of a heat affected zone having less tensile strength and stiffness to less than 1 μm and with reduced grain enlargement. The present invention provides such a bond for electronic packaging of increased reliability, potential functionality, increased manufacturing yield and reduced process complexity.

104. Method/structure for creating aluminum wirebond pad on copper BEOL

United States Patent US6187680

Feb 13, 2001

Inventors: Gregory Costrini, Ronald Dean Goldblatt, John Edward Heidenreich, III, Thomas Leddy McDevitt

Original Assignee: International Business Machines Corporation

Abstract: The present invention provides a method for fabricating an integrated circuit (IC) structure having an Al contact in electrical communication with Cu wiring embedded in the initial semiconductor wafer. In accordance with the method of the present invention, the Al contact is formed in areas of the IC structure which contain or do not contain an underlying region of Cu wiring. The present invention also provides a method of interconnecting the fabricated structure to a semiconducting packaging material through the use of a wirebond or Controlled Collapse Chip Connection (C4) solder.

105. Copper wire-bonding pad

United States Patent US6274935

Aug 14, 2001

Inventor: Cyprian E. Uzoh

Original Assignee: International Business Machines Corporation

Abstract: A copper-containing, wire-bonding pad structure for bonding to gold wires. The structure includes a nickel-containing film to improve metallurgical characteristics. The structure also has a laminated impurity film within the copper pad, which complexes with the nickel-containing pad to prevent a destructive interaction between nickel and copper at elevated temperatures, or during the lifetime of the device or the wirebond.

106. Copper wire-bonding pad

United States Patent US6329722

Dec 11, 2001

Inventors: Wei-Yan Shih, Arthur Wilson, Willmar Subido

Original Assignee: Texas Instruments Incorporated

Abstract: A device having a thin metallic coating, such as tin which forms strong bonds to copper is provided on the bond pads of an integrated circuit having copper metallization; surface oxidation of the coating is self-limiting and the oxides are readily removed; further, the coated bond pad forms intermetallics at low temperatures making it both solderable and compatible with wire bonding. A low cost process for forming tin coated copper bonding pads is provided by electroless plating.

107. Method for enabling conventional wire bonding to copper-based bond pad features

United States Patent US6358847

Mar 19, 2002

Inventors: Hugh Li, Diane J. Hymes

Original Assignee: Lam Research Corporation

Abstract: A method is described comprising removing an oxide from a surface and then commencing application of a passivation layer to the surface within 5 s of the oxide removal. The surface may be a copper surface which may further comprise a bonding pad surface. Removing the oxide may further comprise applying a solution comprising citric acid or hydrochloric acid. Applying the passivation layer may further comprise applying a solution comprising a member of the azole family where the azole family member may further comprise BTA. The method may also further comprise completely applying the passivation layer 35 s after commencing its application.

108. QFN semiconductor package

United States Patent US6459148

Oct 1, 2002

Inventors: Su Chun-Jen, Lin Chien-Tsun, Chang Chao-Chia, Su Yu-Hsien, Tseng Ming-Hui**Original Assignee:** Walsin Advanced Electronics Ltd.

Abstract: A QFN semiconductor package comprises a semiconductor die, a lead frame, bonding wires and a molding compound. The die has an upward topside with a plurality of bonding pads. The lead frame consists of a plurality of inner leads, wherein each inner lead is divided into the front finger portion, the middle protruding portion and the rare connecting portion. The front finger portion is the position of the inner lead to which a bonding wire wire-bonds from the bonding pad of the die. The rare connecting portion is for the electrical out-connection of the package. The middle protruding portion is at height level higher than the front finger portion and the rare connecting portion. The bonding wires electrically connect the bonding pads of the die with the front finger portions of inner leads by means of wire-bonding. A molding compound seals off at least said bonding wires and at least exposes the downside of the die and some surface of the rare connecting portion of each inner lead.

109. Metal redistribution layer having solderable pads and wire bondable pads

United States Patent US6511901

Jan 23, 2003

Inventors: Ken M. Lam, Julius A. Kovats**Original Assignee:** Atmel Corporation

Abstract: A redistribution metallization scheme combines solder bumps and wire bond pads in addition to existing bond pads to enhance the connectivity of a semiconductor device, especially in flip-chip applications. The fabrication method includes forming the additional bond pads during the redistribution deposition step. The metals used in the redistribution layer provide a solderable surface for solder bumping and a bondable surface for wire bonding.

110. Method of improving copper interconnects of semiconductor devices for bonding

United States Patent US6544880

Apr 8, 2003

Inventor: Salman Akram**Original Assignee:** Micron Technology, Inc.

Abstract: An improved wire bond with the bond pads of semiconductor devices and the lead fingers of lead frames or an improved conductor lead of a TAB tape bond with the bond pad of a semiconductor device. More specifically, an improved wire bond wherein the bond pad on a surface of the semiconductor device comprises a layer of copper and at least one layer of metal and/or at least a barrier layer of material between the copper layer and one layer of metal on the copper layer to form a bond pad.

111. Modified pad for copper/low-k

United States Patent US6560862

May 13, 2003

Inventors: Sheng-Hsiung Chen, Shun Long Chen, Hungtse Lin

Original Assignee: Taiwan Semiconductor Manufacturing Company

Abstract: A method to fabricate a bonding pad structure including the following steps. A substrate having a top metal layer and a passivation layer overlying the top metal layer is provided. The top metal layer being electrically connected to a lower metal layer by at least one metal via within a metal via area. The substrate includes a low-*k* dielectric layer at least between the lower metal layer and the top metal layer. The passivation layer is etched within the metal via area to form a trench exposing at least a portion of the top metal layer. A patterned, extended bonding pad is formed over the etched passivation layer and lining the trench. The extended bonding pad having a portion that extends over a peripheral planar area of the substrate adjacent the trench not within the metal via area. A wire bond is bonded to the extended bonding pad at the peripheral planar area portion to form the bonding pad structure.

112. Combined system, method and apparatus for wire bonding and testing

United States Patent US6564115

May 13, 2003

Inventor: Clark Kinnaird

Original Assignee: Texas Instruments Incorporated

Abstract: A combined system and method for computer-controlled bonding and testing of wire connections between integrated circuit chips and substrates, and for automatically adjusting the bonding parameters in response to said testing, comprising the steps of forming a wire connection between said chip and said substrate under computer control to create wire attachments and a wire span; testing said wire connection automatically under computer control to generate test data; and automatically adjusting the bonding parameters of subsequent wire connections responsive to said test data, whereby the number of faulty bonds is reduced to near zero and bonding production downtime is substantially eliminated.

113. Method of preparing copper metallization die for wirebonding

United States Patent US6693020

Feb 17, 2004

Inventors: Kok Wai Mui, Fuaida Bte Harun, Lan Chu Tan, Mohd Faizairi Bin Mohd Nor

Original Assignee: Motorola, Inc.

Abstract: A method of preparing a semiconductor wafer having a integrated circuits formed on it that have pads formed of copper includes the steps of removing oxide from the copper pads and then the vacuum packing the wafer in a shock-proof container. The oxide may be removed from the copper pads in a number of ways. A first way includes cleaning the wafer in an alkaline solution, performing acid neutralization on the cleaned wafer, and then drying the wafer. A second way includes cleaning the wafer with an acid solution, rinsing the acid cleaned wafer with water, applying an anti-oxidant activator to the surface of the copper pads, rinsing the wafer with water after the application of the anti-oxidant activator, and then drying the water rinsed wafer. Yet a third way includes plasma cleaning the copper pads using a combination of about 5–10 % hydrogen and about 90–95 % argon and then sputtering a very thin layer of aluminum on a surface of the copper pads. The layer of aluminum has a thickness of 1–5 nm.

114. Wire bonding process for copper-metallized integrated circuits

United States Patent US6800555

Oct 5, 2004

Inventors: Howard R. Test, Gonzalo Amador, Willmar E. Subido**Original Assignee:** Texas Instruments Incorporated

Abstract: A robust, reliable and low-cost metal structure and process enabling electrical wire/ribbon connections to the interconnecting copper metallization of integrated circuits. The structure comprises a layer of barrier metal that resists copper diffusion, deposited on the non-oxidized copper surface in a thickness such that the barrier layer reduces the diffusion of copper at 250 °C. by more than 80 % compared with the absence of the barrier metal. The structure further comprises an outermost bondable layer which reduces the diffusion of the barrier metal at 250 °C. by more than 80 % compared with the absence of the bondable metal. Finally, a metal wire is bonded to the outermost layer for metallurgical connection.

115. Wire bonding for thin semiconductor package

United States Patent US6815836

Nov 9, 2004

Inventor: Kazuaki Ano**Original Assignee:** Texas Instruments Incorporated

Abstract: An assembly of a semiconductor chip having an integrated circuit (IC) including at least one contact pad on its surface, wherein the contact pad has a metallization suitable for wire bonding, and an interconnect bonded to said contact pad. This interconnect includes a wire attached to the pad by ball bonding, a loop in the wire closed by bonding the wire to itself near the ball, and a portion of the remainder of the wire extended approximately parallel to the surface. The interconnect can be confined to a space equal to or less than three ball heights from the surface.

116. Method of improving copper interconnects of semiconductor devices for bonding

United States Patent US6835643

Dec 28, 2004

Inventor: Salman Akram**Original Assignee:** Micron Technology, Inc.

Abstract: An improved wire bond with the bond pads of semiconductor devices and the lead fingers of lead frames or an improved conductor lead of a TAB tape bond with the bond pad of a semiconductor device. More specifically, an improved wire bond wherein the bond pad on a surface of the semiconductor device comprises a layer of copper and at least one layer of metal and/or at least a barrier layer of material between the copper layer and one layer of metal on the copper layer to form a bond pad.

117. Semiconductor multi-package module having wire bond interconnect between stacked packages

United States Patent US6838761

Jan 4, 2005

Inventor: Marcos Karnezos**Original Assignee:** ChipPAC, Inc.

Abstract: A semiconductor multi-package module having stacked lower and upper packages, each package including a die attached to a substrate, in which the upper and lower substrates are interconnected by wire bonding. Also, a method for making a semiconductor multi-package module, by providing a lower molded package including a lower substrate and a die, affixing an upper molded package including an upper substrate onto the upper surface of the lower package, and forming wire bond z-interconnects between the upper and lower substrates.

118. Semiconductor device having a wire bond pad and method therefor

United States Patent US6846717

Jan 25, 2005

Inventors: Susan H. Downey, James W. Miller, Geoffrey B. Hall

Original Assignee: Freescale Semiconductor, Inc.

Abstract: An integrated circuit has a wire bond pad. The wire bond pad is formed on a passivation layer over active circuitry and/or electrical interconnect layers of the integrated circuit. The wire bond pad is connected to a plurality of final metal layer portions. The plurality of final metal layer portions are formed in a final interconnect layer of the interconnect layers. In one embodiment, the bond pad is formed from aluminum and the final metal layer pads are formed from copper. The wire bond pad allows routing of conductors in a final metal layer directly underlying the bond pad, thus allowing the surface area of the semiconductor die to be reduced.

119. Semiconductor multi-package module having wire bond interconnect between stacked packages

United States Patent US7064426

Jun 20, 2006

Inventor: Marcos Karnezos

Original Assignee: ChipPAC, Inc.

Abstract: A semiconductor multi-package module having stacked lower and upper packages, each package including a die attached to a substrate, in which the upper and lower substrates are interconnected by wire bonding. Also, a method for making a semiconductor multi-package module, by providing a lower molded package including a lower substrate and a die, affixing an upper molded package including an upper substrate onto the upper surface of the lower package, and forming z-interconnects between the upper and lower substrates.

120. Semiconductor chip capable of implementing wire bonding over active circuits

United States Patent US7208837

Apr 24, 2007

Inventors: Kun-Chih Wang, Bing-Chang Wu

Original Assignee: United Microelectronics Corp.

Abstract: A reinforced bonding pad structure includes a bondable metal layer defined on a stress-buffering dielectric layer, and an intermediate metal layer damascened in a first inter-metal dielectric (IMD) layer disposed under the stress-buffering dielectric layer. The intermediate metal layer is situated directly under the bondable metal layer and is electrically connected to the bondable metal layer with a plurality of via plugs integrated with the bondable metal layer. A metal frame

is damascened in a second IMD layer under the first IMD layer. The metal frame is situated directly under the intermediate metal layer for counteracting mechanical stress exerted on the bondable metal layer during bonding, when the thickness of said stress-buffering dielectric layer is greater than 0.2 μm , the damascened metal frame may be omitted. An active circuit portion including active circuit components of the integrated circuit is situated directly under the metal frame.

121. Conductive bumps, wire loops, and methods of forming the same

United States Patent 8152046

Apr 10, 2012

Inventors: Gary S. Gillotti

Assignee: Kulicke and Soffa Industries Inc., Fort Washington, PA (US)

Abstract: A method of forming a conductive bump is provided. The method includes the steps of: (1) bonding a free air ball to a bonding location using a bonding tool to form a bonded ball; (2) raising the bonding tool to a desired height, with a wire clamp open, while paying out wire continuous with the bonded ball; (3) closing the wire clamp; (4) lowering the bonding tool to a smoothing height with the wire clamp still closed; (5) smoothing an upper surface of the bonded ball, with the wire clamp still closed, using the bonding tool; and (6) raising the bonding tool, with the wire clamp still closed, to separate the bonded ball from wire engaged with the bonding tool.

References on Copper Wire Bonding Patents

- [1] Shinichi Terashima, Shinichi Terashima, Tomohiro Uno, Tomohiro Uno, Takashi Yamada, Takashi Yamada, Daizo Oda, Bonding wire for semiconductor, 20120118610, May 17, 2012
- [2] Jie Yang, Qingchin He, Hanmin Zhang, Brace for long wire bond, 20120145446, June 14, 2012
- [3] François Hébert, Arup Bhalla, Copper bonding compatible bond pad structure and method, 20120064711, Mar, 15, 2012
- [4] Francois Hebert, Anup Bhalla, Copper Bonding Method, 8148256, Apr 3, 2012
- [5] Yan Xun Xue, Yan Xun Xue, Jun Lu, Anup Bhalla, Method of making a copper wire bond package, 20120164794, Jun 28, 2012
- [6] Jeng: Yeau-Ren, Wang: Chang-Ming, Method of thermosonic wire bonding process for copper connection in a chip, 6886735
- [7] Wei Qin, Jon W. Brunner, Paul A, Methods of forming wire bonds for wire loops and conductive bumps, 20120074206, Mar 29, 2012
- [8] Isao Araki, Hitachikaminakaishataku Toshio, No. D-101 Chuma, Kazuo Hatori, Masahiro Koizumi, Makoto Nakajima, Yosho Ohashi, Susumu Okikawa, Jin Onuki, Hitoshi Suzuki, Wire bonding, EP0276564 A1, US4976393, EP0276564 B1, Aug 3, 1988, Dec 11, 1990, Mar 11, 1992
- [9] Yasuji Fujii and 3 more, Fine copper wire for electronic instruments and method of manufacturing the same, EP0296596 A1, Dec 28, 1988
- [10] Gonzalo Amador, Willmar E. Subido, Howard R. Test, Wire bonding process, EP1139413 A2, EP1139413 B1, Oct 4, 2001, Mar 16, 2005

- [11] Keiichi Kimura, Tomohiro Uno, Takashi Yamada, Bonding wire for semiconductor devices, EP2200076 A1, Jun 23, 2010
- [12] Keiichi Kimura, Tomohiro Uno, Takashi Yamada, Bonding wire for semiconductor device, EP2239766 A1, Oct 13, 2010
- [13] Keiichi Kimura, Akihito NISHIBAYASHI, Shinichi Terashima, Tomohiro Uno, Takashi Yamada, Semiconductor device bonding wire and wire bonding method, EP2221861 A1, Aug 25, 2010
- [14] Pang Ling Hiew, Christoph Laumen, Method of and device for wire bonding with onsite gas generator, EP2308632 A1, Apr 13, 2011
- [15] Keiichi Kimura, Akihito NISHIBAYASHI, Shinichi Terashima, Tomohiro Uno, Takashi Yamada, Semiconductor device bonding wire, EP2312628 A2, Apr 2011
- [16] Kiyooki Tsumura, Semiconductor device with copper wire ball bonding, 5023697, Jun 11, 1991
- [17] Battista Vitali, Alessandro Frontero, Capillary for bonding copper wires between a semiconductor circuit chip and a corresponding terminal connector of a semiconductor device, 6581816, Jun 24, 2003
- [18] Tomohiro Uno, Keiichi Kimura, Takashi Yamada, Copper alloy bonding wire for semiconductor device, 8004094, Aug 23, 2011
- [19] Keiichi Kimura, Akihito Nishibayashi, Shinichi Terashima, Tomohiro Uno, Takashi Yamada, Wire bonding structure and method for forming same, US8247911 B2, Aug 21, 2012
- [20] Ronaldo Cayetano Calderon, Kian Teng Eng, Yong Chuan Koh, Rodel Manalac, Pang Hup Ong, Jr. Lope Vallespin Pepito, Jeffrey Nantes Salamat, Jimmy Siat, Copper on organic solderability preservative (OSP) interconnect and enhanced wire bonding process, US8247272 B2, Aug 21, 2012
- [21] Dominick A. DeAngelis, Gary W. Schulze, Ultrasonic transducers for wire bonding and methods of forming wire bonds using ultrasonic transducers, US8251275 B2, Aug 28, 2012
- [22] Byung Joon Han and 2 More, Wire bonding structure and method that eliminates special wire bondable finish and reduces bonding pitch on substrates, US8269356 B2, Sep 18, 2012
- [23] Anup Bhalla, Jun Lu, Yan Xun Xue, Method of making a copper wire bond package, US8283212 B2, Oct 9, 2012
- [24] Mark Bachman, John Osenbach, Copper pad for copper wire bonding, US 20100052174 A1, Mar 4, 2010
- [25] Takashi Kitazawa, Yasushige Sakamoto, Motoaki Wakui, Semiconductor device and method for producing the same, US 2011/0304046 A1, Dec 15, 2011
- [26] Shingo Itoh, Shinichi Zenbutsu, Epoxy resin composition for semiconductor encapsulation, cured product thereof, and semiconductor device, US20120261807 A1, Oct 18, 2012
- [27] Tomohiro Uno, Keiichi Kimura, Shinichi Terashima, Takashi Yamada, Akihito Nishibayashi, Semiconductor device bonding wire and wire bonding method, 8102061, Jan 24, 2012
- [28] HanLung Tsai, ChihMing Huang, ChengHsu Hsiao, Semiconductor package using copper wires and wire bonding method for the same, 20080265385, Oct 30, 2010
- [29] Masahiko Sekihara, Takanori Okita, Ultrasonic Wire Bonding Method for a Semiconductor Device, 20120164795, Jun 28, 2012
- [30] Tsumura Kiyooki, Semiconductor device with copper wire ball bonding, 5023697, Jun 1, 1991
- [31] Qwai H. Low, Wire bonding over active circuits, 20090236742, Sep 24, 2009
- [32] Chung Hsing Tzu, Wire bonding structure and manufacturing method thereof, US7859123, Dec 28, 2010

- [33] Ken Pham, Luu T. Nguyen, Wirebonding method and device enabling high speed reverse wedge bonding of wire bonds, 20120032354, Feb 9, 2012
- [34] Hendrik Pieter Hochstenbach, Willem Dirk Van Driel, Eric Ooms, Wirebonding process, 20110192885, Aug 11, 2011
- [35] Donald E. Cousens, John A. Kurtz, Wire bonding technique for integrated circuit chips, EP0073172 A2, Mar 2, 1983
- [36] Osamu C/O Patent Division Usuda, Semiconductor device comprising an electrode pad, EP0271110 A2, EP0271110 A3, EP0271110 B1, Jun 15, 1988, Feb 22, 1989, Oct 6, 1993
- [37] Shigeo Hara, Kazunori Hori, Tokiyuki Seto, Minoru Taguchi, Ultrasonic wire bonding method, EP0286031 A2, Oct 12, 1988
- [38] T. Jeffrey Borenstein, C. Ronald Gonsiorawski, J. Michael Kardauskas, Method of soldering a copper wire to a silver contact on a silicon photovoltaic cell and application of said method to a plurality of silicon photovoltaic cells, EP0503015 B1, Jul 11, 2001
- [39] Hans-Joachim Barth, Cu-pad bonded to Cu-wire with self-passivating Cu-alloys, EP1348235 A2, Oct 1, 2003
- [40] Yakub Aliyu, Simon Chooi, Subhash Gupta, Paul Kwok Keung Ho, Sudipto Ranendra Roy, John Leonard Sudijono, Yi Xu, Mei Sheng Zhou, Pre-cleaning of copper surfaces during Cu/Cu or Cu/Metal bonding using hydrogen plasma, EP1353365 A2, Oct 15, 2003
- [41] Bte Fuaida Harun, Bin Faizairi Mohd Mohd Nor, Wai Kok Mui, Chu Lan Tan, Method of removing oxide from copper bond pads, EP1388167 A2, Feb 11, 2004
- [42] Bte Fuaida Harun, Bin Faizairi Mohd Mohd Nor, Wai Kok Mui, Chu Lan Tan Method of removing oxide from copper bond pads, EP1388167 B1, Aug 23, 2006
- [43] Inc. M. Sumitomo Electric Wintec Fukagaya, Inc. M. Sumitomo Electric Wintec Ioka, S. Sumitomo Electric Ind. Ltd. Kaimori, Inc. T. Sumitomo Electric Wintec Nonaka, Bonding wire, EP1447842 A1, Aug 18, 2004
- [44] Inc. Sumitomo Electric Wintec Masanori Ioka, Osaka Works Sumitomo Elect. Ind. Ltd. S. Kaimori, Inc. Sumitomo Electric Wintec Tsuyoshi Nonaka, Bonding wire and integrated circuit device using the same, EP1677345 A1, Jul 5, 2005
- [45] Albrecht Bischoff, Heinz Förderer, Frank Krüger, Lutz Schräpler, Copper bonding or superfine wire with improved bonding and corrosion properties, EP1856736 A1, Nov 21, 2007
- [46] Yuichiro Nippon Mining & Metals Co. Ltd. , SHINDO, Kouichi Nippon Mining & Metals Co. Ltd., TAKEMOTO Assignee: Nippon Mining & Metals Co., Ltd., Ultrahigh-purity copper and process for producing the same, and bonding wire comprising ultrahigh-purity copper, EP1903119 A1, Mar 26, 2008
- [47] Alfred Steven Kummerl, P. Bernhard Lange, Wire bonding capillary apparatus and method, EP1904264 B1, Aug 10 , 2011
- [48] Yumi Hayashi, Noriaki Matsunaga, Takamasa Usui, Semiconductor device and method for fabricating semiconductor device, US7936070, May 3, 2011
- [49] Qinghuan Sun, Optoelectronic device, US20090127579, May 21, 2009
- [50] Tan Xiaochun, Li Yunfang, Quad flat no-lead (QFN) chip package assembly apparatus and method, US7402459, Jul 22, 2008
- [51] Lloyd G. Burrell, Charles R. Davis, Ronald D. Goldblatt, William F. Landers, Sanjay C. Mehta, Method of fabricating a wire bond pad with Ni/Au metallization, US7294565, Jul 22, 2008
- [52] Kiyoaki Tsumura, Semiconductor device with a copper wires ball bonded to aluminum electrodes, US5229646, Jul 20, 1993
- [53] Kejun Zeng, Wei Qun Peng, Corrosion-resistant copper-to-aluminum bonds, US20120001336, Jan 5, 2012

- [54] Shiro Kobayashi, Masahiko Itoh, Akira Minato, Resin packaged semiconductor device having a protective layer made of a metal-organic matter compound, US4821148, Apr 11, 1989
- [55] Shinichi Zenbutsu (Shinagawa-Ku, JP), Active solid-state devices (e.g., transistors, solid-state diodes) lead frame with structure for mounting semiconductor chip to lead frame (e.g., configuration of die bonding flag, absence of a die bonding flag, recess for led), US4821148, Jul 12, 2012
- [56] Fuaida Harun, Kong Bee Tiu, Wirebonding insulated wire, US6854637, Jul 20, 1993
- [57] Kazuyuki Misumi, Hideyuki Arakawa, Shunji Yamauchi, Mitsuru Aoki, Method of manufacturing semiconductor device, and wire bonder, 20100203681, Aug 12, 2010
- [58] Seok Mo Kwon, Si Hyun Choe, Two step wire bond process, US6461898, Oct 8, 2002
- [59] Allen McTeer, Copper interconnect for an integrated circuit and methods for its fabrication, US6373137, Apr 16, 2002
- [60] Noriyuki Kimura, Manufacturing method for resin sealed semiconductor device, US7271035, Sep 18, 2007
- [61] Tadaaki Ono, Electrode structure of a semiconductor device which uses a copper wire as a bonding wire, US5293073, Mar 8, 1994
- [62] Hiroyasu Itou, Power composite integrated semiconductor device and manufacturing method thereof, US7416932, Aug 26, 2008
- [63] Kiyoaki Tsumura, Method of producing semiconductor device, US5116783, May 26, 1992
- [64] Jutaro Kotani, Masahiro Ihara, Hideaki Nakura, Masami Yokozawa, Semiconductor device including an electrode, US5298793, Mar 29, 1994
- [65] Wan-Kyoon Choi, Jong-Whan Kim, Anti-oxidation system of a wire bonder using a copper wire, US4995552, Feb 26, 1991
- [66] Roberto Tiziani, Loic Renard, Battista Vitali, Semiconductor electronic device and method of manufacturing thereof, US20040072396, May 29, 2003
- [67] Ian Bentley, Alistair D. Bradley, Pressure sense die pad layout and method for direct wire bonding to programmable compensation integrated circuit die, US7677109, Mar 16, 2010
- [68] Masaki Ota, Semiconductor device using bonding wires of different materials, US5173762, Dec 22, 1992
- [69] John A. Fitzsimmons, Jeffrey P. Gambino, Erick G. Walton, Roughened bonding pad and bonding wire surfaces for low pressure wire bonding, US7015580, Mar 21, 2006
- [70] Jitsuho Hirota, Kazumichi Machida, Masaaki Shimotomai, Method of producing a wire bonding ball, US4739142, Apr 19, 1988
- [71] Masatoshi Yasunaga, Hironori Matsushima, Kenya Hironaga, Soshi Kuroda, Semiconductor device, US20110074019, March 31, 2011
- [72] Sang-do Lee, Yong-suk Kwon, Jong-jin Shin, Semiconductor package having oxidation-free copper wire, US20030173659, September 18, 2003
- [73] Noriyuki Kimura, Manufacturing method for resin sealed semiconductor device, US7550322, Jun 23, 2009
- [74] Gary S. Gillotti, Stanley Szczesniak, Peter J. Van Emmerik, Gas delivery system for reducing oxidation in wire bonding operations, US8066170, Nov 29, 2011
- [75] Masahiko Sekihara, Takanori Okita, Ultrasonic wire bonding method for a semiconductor device, US20120164795, June 28, 2012
- [76] Seok Mo Kwon, Si Hyun Choe, Two step wire bond process, US6165888, Dec 26, 2000
- [77] Mei Sheng Zhou, Sangki Hong, Simon Chooi, Aluminum and copper bimetallic bond pad scheme for copper damascene interconnects, US6376353, Apr 23, 2002
- [78] Naoyuki Hosoda, Masaki Morikawa, Naoki Uchiyama, Hideaki Yoshida, Toshiaki Ono, Wire for bonding a semiconductor device, US4717436, Jan 5, 1988

- [79] John Leonard Sudijono, Yakub Aliyu, Mei Sheng Zhou, Simon Chooi, Subhash Gupta, Sudipto Ranendra Roy, Paul Kwok Keung Ho, Yi Xu, Method of using hydrogen plasma to pre-clean copper surfaces during Cu/Cu or Cu/metal bonding, US6720204, Jan 5, 1988
- [80] Kiyoaki Tsumura, Hitoshi Fujimoto, Structure of electrode junction for semiconductor device, US5003373, Mar 26, 1991
- [81] Kwok Keung Paul Ho, Simon Chooi, Yi Xu, Mei Sheng Zhou, Yakub Aliyu, John Leonard Sudijono, Subhash Gupta, Sudipto Ranendra Roy, Method of application of copper solution in flip-chip, COB, and micrometal bonding, US6415973, Jul 9, 2002
- [82] Qwai H. Low, Wire bonding over active circuits, US8125091, Feb 28, 2012
- [83] Jeffrey Alan Brigante, Zhong-Xiang He, Barbara Ann Waterhouse, Eric Jeffrey White, Low cost bonding pad and method of fabricating same, US7245025, Jul 17, 2007
- [84] Loon A Lim, Charles J Vath, III, Capillary for wire bonding, US7427009, Sep 23, 2008
- [85] Yong Chuan Koh, Jimmy Siat, Jeffrey Nantes Salamat, Lope Vallespin Pepito, Jr., Ronaldo Cayetano Calderon, Rodel Manalac, Pang Hup Ong, Kian Teng Eng, Copper on organic solderability preservative (OSP) interconnect and enhanced wire bonding process, US20100025849, Feb 4, 2010
- [86] Wen-Lo Shieh, Ning Huang, Hui-Pin Chen, Hua-Wen Chiang, Chung-Ming Chang, Feng-Chang Tu, Fu-Yu Huang, Hsuan-Jui Chang, Chia-Chieh Hu, Wen-Long Leu, Fabrication method of semiconductor, US20030059721, Mar 27, 2003
- [87] Tomohiro Uno, Shinichi Terashima, Keiichi Kimura, Takashi Yamada, Akihito Nishibayashi, Bonding structure of bonding wire and method for forming same, US20100213619, Aug 26, 2010
- [88] Naoyuki Hosoda, Masaki Morikawa, Naoki Uchiyama, Hideaki Yoshida, Toshiaki Ono, Wire for bonding a semiconductor device and process for producing the same, US4676827, Jun 30, 1987
- [89] Kian Teng Eng, Wolfgang Johannes Hetzel, Werner Josef Reiss, Florian Ammer, Yong Chuan Koh, Jimmy Siat, Copper on organic solderability preservative (OSP) interconnect, US20090008796, Jan 8, 2009
- [90] Osamu Usuda, Semiconductor device having improved electrode pad structure, US5060051, Oct 22, 1991
- [91] Sinji Sibata, Shuji Sakou, Akihiko Ogino, Wire bonding apparatus and method, US5452841, Sep 26, 1995
- [92] Satoshi Onai, Minoru Akaishi, Hiroshi Ishizeki, Yoshiaki Sano, Original Assignees: Semiconductor Components Industries, Llc, Sanyo Semiconductor Co., Ltd., Semiconductor device and method of manufacturing the same, US8227341, Jul 24, 2012
- [93] Albrecht Bischoff, Heinz Förderer, Lutz Schröpler, Frank Krüger, Copper bonding or superfine wire with improved bonding and corrosion properties, US7645522, Jan 12, 2010
- [94] Jin-Ho Kim, In-Ku Kang, Sang-Yeop Lee, Wire bonding method, semiconductor chip, and semiconductor package, US7067413, Jun 27, 2006
- [95] Rudolph M. Wicen, Supplying a cover gas for wire ball bonding, US6234376, May 22, 2001
- [96] Tomohiro Uno, Keiichi Kimura, Takashi Yamada, Copper alloy bonding wire for semiconductor device, US8004094, Aug 23, 2001
- [97] Ming-Tao Chung, Fu-Yuan Hsieh, Trench MOSFET with trench source contact havingcopper wire bonding, US20100127323, Nov 26, 2008
- [98] Sang-do Lee, Yong-suk Kwon, Jong-jin Shin, Semiconductor package having oxidation-free copper wire, 20030173659, Sep 18, 2003
- [99] Kiyoaki Tsumura, Semiconductor device with copper wire ball bonding, US5023697, Jun 11, 1991
- [100] Robin.W.Cheung, Ming-Ren Lin, Advanced copper interconnect system that is compatible with existing IC wire bonding technology, US5785236, Jul 28, 1998

- [101] Chi-Cheong Shen, Donald C. Abbott, Walter Bucksch, Marco Corsi, Taylor Rice Efland, John P. Erdeljac, Louis Nicholas Hutter, Quang Mai, Konrad Wagensohner, Charles Edward Williams, Integrated circuit with bonding layer over active circuitry, US6144100, Nov 7, 2000
- [102] Gregory M. Chapman, Michael J. Bettinger, Jennifer A. Due, Concave face wire bond capillary, US6158647, Dec 12, 2000
- [103] Nikhil M. Murdeshwar, Control of size and heat affected zone for fine pitch wire bonding, US6180891, Jan 30, 2001
- [104] Gregory Costrini, Ronald Dean Goldblatt, John Edward Heidenreich, III, Thomas Leddy McDevitt, Method/structure for creating aluminum wirebound pad on copper BEOL, US6187680, Feb 13, 2001
- [105] Cyprian E. Uzoh, Copper wire-bonding pad, US6274935, Aug 14, 2001
- [106] Wei-Yan Shih, Arthur Wilson, Willmar Subido, Copper wire-bonding pad, US6329722, Dec 11, 2001
- [107] Hugh Li, Diane J. Hymes, Method for enabling conventional wire bonding to copper-based bond pad features, US6358847, Mar 19, 2002
- [108] Su Chun-Jen, Lin Chien-Tsun, Chang Chao-Chia, Su Yu-Hsien, Tseng Ming-Hui, QFN semiconductor package, US6459148, Oct 1, 2002
- [109] Ken M. Lam, Julius A. Kovats, Metal redistribution layer having solderable pads and wire bondable pads, US6511901, Jan 23, 2003
- [110] Salman Akram, Method of improving copper interconnects of semiconductor devices for bonding, US6544880, Apr 8, 2003
- [111] Sheng-Hsiung Chen, Shun Long Chen, Hungtse Lin, Modified pad for copper/low-k, US6560862, May 13, 2003
- [112] Clark Kinnaird, Combined system, method and apparatus for wire bonding and testing, US6564115, May 13, 2003
- [113] Kok Wai Mui, Fuaida Bte Harun, Lan Chu Tan, Mohd Faizairi Bin Mohd Nor, Method of preparing copper metallization die for wirebonding, US6693020, Feb 17, 2004
- [114] Howard R. Test, Gonzalo Amador, Willmar E. Subido, Wire bonding process for copper-metallized integrated circuits, US6800555, Oct 5, 2004
- [115] Kazuaki Ano, Wire bonding for thin semiconductor package, US6815836, Nov 9, 2004
- [116] Salman Akram, Method of improving copper interconnects of semiconductor devices for bonding, US6835643, Dec 28, 2004
- [117] Marcos Kamezos, Semiconductor multi-package module having wire bond interconnect between stacked packages, US6838761, Jan 4, 2005
- [118] Susan H. Downey, James W. Miller, Geoffrey B. Hall, Semiconductor device having a wire bond pad and method therefor, US6846717, Jan 25, 2005
- [119] Marcos Kamezos, Semiconductor multi-package module having wire bond interconnect between stacked packages, US7064426, Jun 20, 2006
- [120] Kun-Chih Wang, Bing-Chang Wu, Semiconductor chip capable of implementing wire bonding over active circuits, US7208837, Apr 24, 2007
- [121] Gary S. Gillotti, Conductive bumps, wire loops, and methods of forming the same, 8152046, Apr 10, 2012

References

1. J. Pan and P. Fraud, "Wire bonding challenges in optoelectronics packaging," *Proceedings of the 1st SME Annual Manufacturing Technology Summit: Dearborn, MI*, 2004.
2. G. Ginsberg, *Surface Mount and Related Technologies* vol. 57: CRC, 1989.
3. E. Kim, "Wire bonding techniques," 2004.
4. B. Langenecker, "Effects of ultrasound on deformation characteristics of metals," *Sonics and Ultrasonics, IEEE Transactions on*, vol. 13, pp. 1–8, 1966.
5. M. Tarr, "Bonding to the chip face."
6. Z. W. Zhong, "Overview of wire bonding using copper wire or insulated wire," *Microelectronics Reliability*, vol. 51, pp. 4–12, 2011.
7. C. QiJia, A. Pagba, D. Reynoso, S. Thomas, and H. J. Toc, "Cu wire and beyond - Ag wire an alternative to Cu?," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 591-596.
8. J. Sylvester, "Comparing Au, Pt, Ag and Cu wire bonding," in *PTI Blog*, ed, 2013.
9. *Gold monthly price - US dollars per troy ounce*. Available: <http://www.indexmundi.com/commodities/?commodity=gold&months=60>
10. G. Hu, "Comparison of copper, silver and gold wire bonding on interconnect metallization," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2012 13th International Conference on*, 2012, pp. 529-533.
11. Q. Chen, A. Pagba, D. Reynoso, and S. Thomas, "Cu wire and beyond-Ag wire an alternative to Cu?," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 591-596.
12. K. A. Yoo, C. Uhm, T. J. Kwon, J. S. Cho, and J. T. Moon, "Reliability study of low cost alternative Ag bonding wire with various bond pad materials," in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 851-857.
13. L. J. Kai, L. Y. Hung, L. W. Wu, M. Y. Chiang, D. S. Jiang, C. Huang, and Y. P. Wang, "Silver alloy wire bonding," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 1163–1168.
14. (2013). *Copper, grade A cathode monthly price - US dollars per metric ton*. Available: <http://www.indexmundi.com/commodities/?commodity=copper&months=60>
15. H. K. Kung and H. S. Chen, "The equivalent diameter of copper wire and gold wire based on the sweep stiffness evaluation in semiconductor packaging," in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 21–26.
16. T. K. Lee, C. D. Breach, and W. L. Chong, "Comparson of Au/Al and Cu/Al in wirebonding assembly and reliability," in *Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2011 6th International*, 2011, pp. 234–237.

17. L. Hung, Y. Lin, S. Chen, Y. Wang, and C. S. Hsiao, "The characterization of intermetallic growth in copper and gold ball bonded on thicker aluminum," in *Electronic Packaging Technology, 2006. ICEPT '06. 7th International Conference on*, 2006, pp. 1–6.
18. M. Deley and L. Levine, "The emergence of high volume copper ball bonding," in *Electronics Manufacturing Technology Symposium, 2004. IEEE/CPMT/SEMI 29th International*, 2004, pp. 186–190.
19. S. Zhang, C. Chen, R. Lee, A. K. M. Lau, P. P. H. Tsang, L. Mohamed, C. Y. Chan, and M. Dirkzwager, "Characterization of intermetallic compound formation and copper diffusion of copper wire bonding," in *Electronic Components and Technology Conference, 2006. Proceedings. 56th*, 2006, p. 6.
20. Y. Jiang, R. Sun, Y. Yu, and Z. Wang, "Study of 6 mil Cu wire replacing 10-15 mil Al wire for maximizing wire-bonding process on power ICs," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 33, pp. 135–142, 2010.
21. C. T. h. Lu, "The challenges of copper wire bonding," in *Microsystems Packaging Assembly and Circuits Technology Conference (IMPACT), 2010 5th International*, 2010, pp. 1–4.
22. F. W. Wulff, C. D. Breach, D. Stephan, Saraswati, and K. J. Dittmer, "Characterisation of intermetallic growth in copper and gold ball bonds on aluminium metallization," in *Electronic Packaging Technology Conference, 2004. EPTC 2004. Proceedings of 6th*, 2004, pp. 348–353.
23. H. Clauberg, P. Backus, and B. Chylak, "Nickel-palladium bond pads for copper wire bonding," *Microelectronics Reliability*, vol. 51, pp. 75–80, Jan 2011.
24. S. Mori, H. Yoshida, and N. Uchiyama, "The development of new copper ball bonding-wire," in *Electronic Components Conference, 1988., Proceedings of the 38th*, 1988, pp. 539–545.
25. F. Y. Hung, Y. T. Wang, L. H. Chen, and T. S. Lui, "Recrystallization effect and electric flame-off characteristic of thin copper wire," *Materials Transactions*, vol. 47, pp. 1776–1781, Jul 2006.
26. F. Y. Hung, T. S. Lui, L. H. Chen, and Y. C. Lin, "Recrystallization, electric flame-off characteristics, and electron backscatter diffraction of copper bonding wires," *IEEE Transactions on Advanced Packaging*, vol. 33, pp. 58–63, Feb 2010.
27. A. Shah, M. Mayer, Y. Zhou, S. J. Hong, and J. T. Moon, "Reduction of underpad stress in thermosonic copper ball bonding," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, 2008, pp. 2123–2130.
28. L. England and T. Jiang, "Reliability of Cu wire bonding to Al metallization," in *Electronic Components and Technology Conference, 2007. ECTC '07. Proceedings. 57th*, 2007, pp. 1604–1613.
29. B. K. Appelt, L. Huang, Y. Lai, and S. Chen, "Three years of fine Cu wire bonding in high volume manufacturing," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*, 2011, pp. 1–3.
30. S. L. Khoury, D. J. Burkhard, D. P. Galloway, and T. A. Schar, "A comparison of copper and gold wire bonding on integrated circuit devices," in *Electronic Components and Technology Conference, 1990. 40th*, 1990, pp. 768–776 vol.1.
31. S. S. H. Teh, B. Y. Low, C. S. Foong, and C. T. Siong, "Wire sweep characterization of multi-tier copper wire bonding on thermally-enhanced plastic ball grid array packages," in *Electronic Manufacturing Technology Symposium (IEMT), 2010 34th IEEE/CPMT International*, 2010, pp. 1–5.
32. S. Inderjit, J. Y. On, and L. Levine, "Enhancing fine pitch, high I/O devices with copper ball bonding," in *Electronic Components and Technology Conference, 2005. Proceedings. 55th*, 2005, pp. 843–847 Vol. 1.
33. H. Clauberg, I. Qin, and B. Chylak. (2010) Fine pitch copper wire bonding. *Chip Scale Review*.
34. Micro-mechanics Limited. (2012, 14 August 2012). *2Q12 results briefing*. Available: <http://www.micro-mechanics.com/>

35. U. Chaudhary, D. Corral, and G. Ryan, "TI's journey to high-volume copper wire bonding production," 2013.
36. MarketWatch, "Texas instruments drives adoption of copper wire bonding technology, delivering nearly 6.5 billion units to customers," 2012.
37. L. C. Matthew, "Developments in copper wire bonding," 2011.
38. M. Hong and J. Shen. (2012, ASE, SPIL make progress in transition to copper wire bonding. Available: <http://www.digitimes.com/news/a20120730PD215.html?mod=3&q=SEMI-CONDUCTOR+>
39. "Fourth quarter 2012 investor conference," 2013.
40. (2013). ASE, SPIL to stop ramping copper wirebonding capacity. Available: <http://en.chinaflashmarket.com/TradeNewsDetails.aspx?QXJ0aWNsZV9JRD0yNTE1>
41. F. Carson, L. Hun Teak, Y. Jae Hak, J. Punzalan, and E. Fontanilla, "Die to die copper wire bonding enabling low cost 3D packaging," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1502–1507.
42. K. Toyozawa, K. Fujita, S. Minamide, and T. Maeda, "Development of copper wire bonding application technology," in *Electronic Components and Technology Conference, 1990. 40th*, 1990, pp. 762–767 vol.1.
43. M. Drozdov, G. Gur, Z. Atzmon, and W. D. Kaplan, "Detailed investigation of ultrasonic Al–Cu wire-bonds: I. Intermetallic formation in the as-bonded state," *Journal of Materials Science*, vol. 43, pp. 6029–6037, 2008.
44. N. Srikanth, J. Premkumar, M. Sivakumar, Y. M. Wong, and C. J. Vath, "Effect of wire purity on copper wire bonding," in *Electronics Packaging Technology Conference, 2007. EPTC 2007. 9th*, 2007, pp. 755–759.
45. M. Schneider-Ramelow, U. Geißler, S. Schmitz, W. Grübl, and B. Schuch, "Development and status of Cu ball/wedge bonding in 2012," *Journal of Electronic Materials*, pp. 1–38, 2013/01/01 2013.
46. Quik-Pak, "Wire Bonding Servies."
47. R. Dohle, M. Petzold, R. Klengel, H. Schulze, and F. Rudolf, "Room temperature wedge–wedge ultrasonic bonding using aluminum coated copper wire," *Microelectronics Reliability*, vol. 51, pp. 97–106, 2011.
48. S. Kaimori, T. Nonaka, and A. Mizoguchi, "The development of Cu bonding wire with oxidation-resistant metal coating," *IEEE Transactions on Advanced Packaging*, vol. 29, pp. 227–231, May 2006.
49. T. Uno, K. Kimura, and T. Yamada, "Surface-enhanced copper bonding wire for LSI and its bond reliability under humid environment," in *Microelectronics and Packaging Conference, 2009. EMPC 2009. European*, 2009, pp. 1–10.
50. T. Uno, "Bond reliability under humid environment for coated copper wire and bare copper wire," *Microelectronics Reliability*, vol. 51, pp. 148–156, Jan 2011.
51. I. Qin, X. Hui, H. Clauberg, R. Cathcart, V. L. Acoff, B. Chylak, and H. Cuong, "Wire bonding of Cu and Pd coated Cu wire: bondability, reliability, and IMC formation," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1489–1495.
52. O. Yauw, H. Clauberg, L. Kuan Fang, S. Liming, and B. Chylak, "Wire bonding optimization with fine copper wire for volume production," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 467–472.
53. N. SeokHo, H. TaeKyeong, P. JungSoo, K. JinYoung, Y. HeeYeoul, and L. ChoonHeung, "Characterization of intermetallic compound (IMC) growth in Cu wire ball bonding on Al pad metallization," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1740–1745.
54. K. Soffa, in *Presentation*, ed, 2012.
55. Z. W. Zhong, H. M. Ho, Y. C. Tan, W. C. Tan, H. M. Goh, B. H. Toh, and J. Tan, "Study of factors affecting the hardness of ball bonds in copper wire bonding," *Microelectronic Engineering*, vol. 84, pp. 368–374, 2007.

56. H.-C. Hsu, W.-Y. Chang, C.-L. Yeh, and Y.-S. Lai, "Characteristic of copper wire and transient analysis on wirebonding process," *Microelectronics Reliability*, vol. 51, pp. 179–186, 2011.
57. T. Tu Anh, L. Chu-Chung, V. Mathew, and L. Higgins, "Copper wire bonding on low-k/copper wafers with bond over active (BOA) structures for automotive customers," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1508–1515.
58. D. Stephan, F. W. Wulff, and E. Milke, "Reliability of palladium coated copper wire," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 343–348.
59. J. Foley, H. Clauberg, and B. Chylak, "Enabling high volume fine pitch copper wire bonding: enhancements to process and equipment capability," in *Electronic System-Integration Technology Conference (ESTC), 2010 3rd*, 2010, pp. 1–4.
60. P. Liu, L. Tong, J. Wang, L. Shi, and H. Tang, "Challenges and developments of copper wire bonding technology," *Microelectronics Reliability*, vol. 52, pp. 1092–1098, 2012.
61. M. H. Hong, J. Tan, C. T. Yee, H. T. Boon, and P. Xavier, "Modeling energy transfer to copper wire for bonding in an inert environment," in *Electronic Packaging Technology Conference, 2005. EPTC 2005. Proceedings of 7th*, 2005, pp. 292–297.
62. C. Hua, S. W. R. Lee, and D. Yutian, "Evaluation of bondability and reliability of single crystal copper wire bonding," in *High Density Microsystem Design and Packaging and Component Failure Analysis, 2005 Conference on*, 2005, pp. 1–7.
63. S.-D. Lee, Kwon, Y.-S., Shin, J.-J., "Semiconductor package having oxidation-free copper wire," 2003.
64. X. Fan, T. Wang, Y. Cong, B. Zhang, and J. Wang, "Oxidation study of copper wire bonding," in *Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), 2010 11th International Conference on*, 2010, pp. 246–249.
65. C. J. Hang, W. H. Song, I. Lum, M. Mayer, Y. Zhou, C. Q. Wang, J. T. Moon, and J. Persic, "Effect of electronic flame off parameters on copper bonding wire: free-air ball deformability, heat affected zone length, heat affected zone breaking force," *Microelectronic Engineering*, vol. 86, pp. 2094–2103, 2009.
66. I. Qin, A. Shah, C. Huynh, M. Meyer, M. Mayer, and Y. Zhou, "Effect of process parameters on pad damage during Au and Cu ball bonding processes," in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 573–578.
67. K. Fujimoto, S. Nakata, T. Manabe, and A. Fujii, "Effects of bonding conditions and surface state on bondability: Study of Cu wire stitch bonding (1st Report)," 1996.
68. B. K. Appelt, A. Tseng, and L. Yi-Shao, "Fine pitch copper wire bonding introduction to high volume production," in *Electronic System-Integration Technology Conference (ESTC), 2010 3rd*, 2010, pp. 1–5.
69. B. K. Appelt, W. T. Chen, A. Tseng, and L. Yi-Shao, "Fine pitch Cu wire bonding- as good as gold," in *CPMT Symposium Japan, 2010 IEEE*, 2010, pp. 1–4.
70. A. Bing, D. Lan, W. Techun, L. Tailieh, and W. Yiping, "Annealing effect and crystallization characteristics of copper wire bonding on pre-plated leadframe," in *Advanced Packaging Materials (APM), 2011 International Symposium on*, 2011, pp. 141–144.
71. H. Huang, A. Pequegnat, B. Chang, M. Mayer, D. Du, and Y. Zhou, "Influence of superimposed ultrasound on deformability of Cu," *Journal of Applied Physics*, vol. 106, pp. 113514–113516, 2009.
72. G. Harman, *Wire bonding in microelectronics, 3rd edition*: McGraw-Hill Companies, Incorporated, 2010.
73. A. Shah, A. Rezvani, M. Mayer, Y. Zhou, J. Persic, and J. T. Moon, "Reduction of ultrasonic pad stress and aluminum splash in copper ball bonding," *Microelectronics Reliability*, vol. 51, pp. 67–74, Jan 2011.
74. I. Lum, C. Hang, M. Mayer, and Y. Zhou, "In Situ Studies of the Effect of Ultrasound During Deformation on Residual Hardness of a Metal," *Journal of Electronic Materials*, vol. 38, pp. 647–654, 2009.

75. Y. Tian, C. Wang, I. Lum, M. Mayer, J. P. Jung, and Y. Zhou, "Investigation of ultrasonic copper wire wedge bonding on Au/Ni plated Cu substrates at ambient temperature," *Journal of Materials Processing Technology*, vol. 208, pp. 179–186, 2008.
76. S. Hong, C. Hang, and C. Wang, "Experimental research of copper wire ball bonding," in *Electronic Packaging Technology, 2005 6th International Conference on*, 2005, pp. 1–5.
77. X. Hui, L. Changqing, V. V. Silberschmidt, and W. Honghui, "Effects of process parameters on bondability in thermosonic copper ball bonding," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, 2008, pp. 1424–1430.
78. H. Clauberg, P. Backus, and B. Chylak, "Nickel–palladium bond pads for copper wire bonding," *Microelectronics Reliability*, vol. 51, pp. 75–80, 2011.
79. S. H. Kim, H. W. Park, and J. T. Moon, "Optimized conditions to make stable free air ball (FAB) for copper bonding wire," in *Electronic Manufacturing Technology Symposium (IEMT), 2008 33rd IEEE/CPMT International*, 2008, pp. 1–2.
80. L.-n. Sun, Y.-t. Liu, and Y.-j. Liu, "Factors governing heat affected zone during wire bonding," *Transactions of Nonferrous Metals Society of China*, vol. 19, Supplement 2, pp. s490–s494, 2009.
81. S. S. Sripada, I. M. Cohen, P. S. Ayyaswamy, L. Medalla, and B. J. Mulada, "Heat affected zone in the wire electrode during electronic flame off in bonding," *International Journal of Microcircuits and Electronic Packaging*, vol. 22, pp. 203–211, 1999.
82. J. L. Chen and Y. C. Lin, "A new approach in free air ball formation process parameters analysis," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 23, pp. 116–122, 2000.
83. W. H. Song, M. Mayer, Y. Zhou, S. H. Kim, J. S. Hwang, and J. T. Moon, "Effect of EFO parameters and superimposed ultrasound on work hardening behavior of palladium coated copper wire in thermosonic ball bonding," *Microelectronics Reliability*.
84. C. J. Hang, C. Q. Wang, Y. H. Tian, M. Mayer, and Y. Zhou, "Microstructural study of copper free air balls in thermosonic wire bonding," *Microelectronic Engineering*, vol. 85, pp. 1815–1819, 2008.
85. A. Pequegnat, H. J. Kim, M. Mayer, Y. Zhou, J. Persic, and J. T. Moon, "Effect of gas type and flow rate on Cu free air ball formation in thermosonic wire bonding," *Microelectronics Reliability*, vol. 51, pp. 43–52, 2011.
86. L. L. Jeng, L. K. Hwa, and N. W. Chang, "Impacts to fine pitch copper wire bonding quality by external airflow," in *Electronic Manufacturing Technology Symposium (IEMT), 2010 34th IEEE/CPMT International*, 2010, pp. 1–5.
87. W. Koh, T. K. Lee, H. S. Ng, K. S. Goh, and H. M. Ho, "Investigation of palladium coverage on bonded balls of palladium-coated copper wires," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*, 2011, pp. 188–194.
88. L. J. Tang, H. M. Ho, W. Koh, Y. J. Zhang, K. S. Goh, C. S. Huang, and Y. T. Yu, "Pitfalls and solutions of replacing gold wire with palladium coated copper wire in IC wire bonding," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1673–1678.
89. Y.-W. Lin, R.-Y. Wang, W.-B. Ke, I. S. Wang, Y.-T. Chiu, K.-C. Lu, K.-L. Lin, and Y.-S. Lai, "The Pd distribution and Cu flow pattern of the Pd-plated Cu wire bond and their effect on the nanoindentation," *Materials Science and Engineering: A*, vol. 543, pp. 152–157, 2012.
90. C. Hang, C. Wang, M. Shi, X. Wu, and H. Wang, "Study of copper free air ball in thermosonic copper ball bonding," in *Electronic Packaging Technology, 2005 6th International Conference on*, 2005, pp. 414–418.
91. Y. Jiang, R. Sun, S. Wang, D. Min, and W. Chen, "Study of a practicable wire bonding method for applying copper wire bond to large-scale integrated circuits," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1169–1165.

92. L. J. Tang, H. M. Ho, Y. J. Zhang, Y. M. Lee, and C. W. Lee, "Investigation of palladium distribution on the free air ball of Pd-coated Cu wire," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 777–782.
93. H. Clauberg, B. Chylak, N. Wong, J. Yeung, and E. Milke, "Wire bonding with Pd-coated copper wire," in *CPMT Symposium Japan, 2010 IEEE*, 2010, pp. 1–4.
94. Z. Chen, Y. Liu, and S. Liu, "Comparison of the copper and gold wire bonding processes for LED packaging," *Journal of Semiconductors*, vol. 32, p. 024011, 2011.
95. Z. Chen, Y. Liu, and S. Liu, "Modeling of copper wire bonding process on high power LEDs," *Microelectronics Reliability*, vol. 51, pp. 171–178, 2011.
96. H. Chu, J. Hu, L. Jin, and Y. Jie, "Defect analysis of copper ball bonding," in *Electronic Packaging Technology & High Density Packaging, 2008. ICEPT-HDP 2008. International Conference on*, 2008, pp. 1–3.
97. J. Lee, M. Mayer, Y. Zhou, S. J. Hong, and J. T. Moon, "Concurrent optimization of crescent bond pull force and tail breaking force in a thermosonic Cu wire bonding process," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 32, pp. 157–163, 2009.
98. H. M. Ho, W. Lam, S. Stoukatch, P. Ratchev, C. J. Vath III, and E. Beyne, "Direct gold and copper wires bonding on copper," *Microelectronics Reliability*, vol. 43, pp. 913–923, 2003.
99. Y. H. Tian, C. J. Hang, C. Q. Wang, G. Q. Ouyang, D. S. Yang, and J. P. Zhao, "Reliability and failure analysis of fine copper wire bonds encapsulated with commercial epoxy molding compound," *Microelectronics Reliability*, vol. 51, pp. 157–165, Jan 2011.
100. E. Spaan, E. Ooms, W. D. van Driel, C. A. Yuan, D. G. Yang, and G. Q. Zhang, "Wire bonding the future: a combined experimental and numerical approach to improve the Cu-wire bonding quality," in *Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE), 2010 11th International Conference on*, 2010, pp. 1–4.
101. B. T. Ng, V. P. Ganesh, and C. Lee, "Optimization of gold wire bonding on electroless nickel immersion gold for high temperature applications," in *Electronics Packaging Technology Conference, 2006. EPTC '06. 8th*, 2006, pp. 277–282.
102. C.-T. Su and C.-J. Yeh, "Optimization of the Cu wire bonding process for IC assembly using taguchi methods," *Microelectronics Reliability*, vol. 51, pp. 53–59, 2011.
103. N. Lin, C. E. Tan, and Y. J. Pan, "Copper wire bonding challenges and solutions of small outline packages," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 603–607.
104. C. C. Lim, Y. C. Soh, C. C. Lee, and O. S. Lim, "Challenges of 43 um Cu bonding on very thin & softest Al bond pad structure," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 37–43.
105. B. K. Wong, C. C. Yong, P. L. Eu, and B. K. Yap, "Process optimization approach in fine pitch Cu wire bonding," in *Electronic Devices, Systems and Applications (ICEDSA), 2011 International Conference on*, 2011, pp. 147–151.
106. M. Sheaffer, L. Levine, and B. Schlain, "Optimizing the wire-bonding process for copper ball bonding, using classic experimental designs," *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on*, vol. 10, pp. 321–326, 1987.
107. S. C. Teck, J. L. L. Tin, L. S. Khoon, and N. K. O. Kalandar, "Ultra fine pitch bare Cu wire bonding manufacturability control for plastic ball grid array device," in *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*, 2011, pp. 304–312.
108. Y. K. Yun and E. P. Leng, "Cu wire bond reliability improvement through focused heat treatment after bonding," in *Electronic Manufacturing Technology Symposium (IEMT), 2008 33rd IEEE/CPMT International*, 2008, pp. 1–7.
109. B. S. Kumar, M. S. R. Malliah, M. Li, Y. Song Keng, and J. James, "Process characterization of Cu & Pd coated Cu wire bonding on overhang die: challenges and solution," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 859–867.

110. J. Li, L. Liu, L. Deng, B. Ma, F. Wang, and L. Han, "Interfacial microstructures and thermodynamics of thermosonic Cu-wire bonding," *Electron Device Letters, IEEE*, vol. 32, pp. 1433–1435, 2011.
111. J. Li, L. Liu, B. Ma, L. Deng, and L. Han, "Dynamics features of Cu-wire bonding during overhang bonding process," *Electron Device Letters, IEEE*, vol. 32, pp. 1731–1733, 2011.
112. C. Inc., "Capillary wirebonding."
113. K. S. Goh and Z. W. Zhong, "A new bonding-tool solution to improve stitch bondability," *Microelectronic Engineering*, vol. 84, pp. 173–179, Jan 2007.
114. M. Sivakumar, V. Kripesh, L. Loon Aik, and M. Kumar, "Fine pitch copper wire bond process development for dual damascene Cu metallized chips," in *Electronics Packaging Technology Conference, 2002. 4th*, 2002, pp. 350–355.
115. C. W. Leong, N. B. Jaafar, M. Chew, S. Sivakumar, G. Gunasekaran, K. Kanchet, D. Witarasa, J. B. Tan, V. R. Srinivasa, T. C. Chai, A. Alastair, and J. Woo, "Fine pitch copper wire bonding on 45 nm tech Cu/low-k chip with different bond pad metallurgy," in *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*, 2011, pp. 752–757.
116. K. S. Goh and Z. W. Zhong, "Two capillary solutions for ultra-fine-pitch wire bonding and insulated wire bonding," *Microelectronic Engineering*, vol. 84, pp. 362–367, Feb 2007.
117. K. S. Goh and Z. W. Zhong, "Development of capillaries for wire bonding of low-k ultra-fine-pitch devices," *Microelectronic Engineering*, vol. 83, pp. 2009–2014, Oct 2006.
118. Z. W. Zhong and K. S. Goh, "Investigation of ultrasonic vibrations of wire-bonding capillaries," *Microelectronics Journal*, vol. 37, pp. 107–113, Feb 2006.
119. C. W. Leong, X. Zhang, V. Kripesh, C. S. Premachandran, S. C. Chong, Y. Y. Liu, J. Madhukumar, V. R. Srinivas, P. P. Thaw, M. J. Jong, J. H. Lau, S. Wang, C. K. Foo, M. L. Thew, E. P. P. Myo, and W. L. Teo, "Reliability results of 0.8 mil fine pitch copper wire bonding on immersion gold plated pad for copper low-k devices," in *Electronics Packaging Technology Conference, 2008. EPTC 2008. 10th*, 2008, pp. 957–964.
120. B. Zhang, K. Qian, T. Wang, Y. Cong, M. Zhao, X. Fan, and J. Wang, "Behaviors of palladium in palladium coated copper wire bonding process," in *Electronic Packaging Technology & High Density Packaging, 2009. ICEPT-HDP '09. International Conference on*, 2009, pp. 662–665.
121. H. Xu, C. Liu, V. V. Silberschmidt, S. S. Pramana, T. J. White, and Z. Chen, "A re-examination of the mechanism of thermosonic copper ball bonding on aluminium metallization pads," *Scripta Materialia*, vol. 61, pp. 165–168, Jul 2009.
122. H. Xu, C. Liu, V. V. Silberschmidt, S. S. Pramana, T. J. White, Z. Chen, M. Sivakumar, and V. L. Acoff, "A micromechanism study of thermosonic gold wire bonding on aluminum pad," *Journal of Applied Physics*, vol. 108, Dec 1 2010.
123. H.-J. Kim, J. Y. Lee, K.-W. Paik, K.-W. Koh, J. Won, S. Choe, J. Lee, J.-T. Moon, and Y.-J. Park, "Effects of Cu/Al intermetallic compound (IMC) on copper wire and aluminum pad bondability," *Components and Packaging Technologies, IEEE Transactions on*, vol. 26, pp. 367–374, 2003.
124. H. Xu, C. Liu, V. Silberschmidt, and Z. Chen, "Growth of intermetallic compounds in thermosonic copper wire bonding on aluminum metallization," *Journal of Electronic Materials*, vol. 39, pp. 124–131, 2010.
125. H. Xu, C. Liu, V. V. Silberschmidt, Z. Chen, and V. L. Acoff, "Effect of ultrasonic energy on nanoscale interfacial structure in copper wire bonding on aluminium pads," *Journal of Physics D-Applied Physics*, vol. 44, Apr 13, 2011.
126. H. Xu, C. Liu, V. V. Silberschmidt, S. S. Pramana, T. J. White, Z. Chen, and V. L. Acoff, "Behavior of aluminum oxide, intermetallics and voids in Cu–Al wire bonds," *Acta Materialia*, vol. 59, pp. 5661–5673, 2011.
127. J. Premkumar, B. S. Kumar, M. Madhu, M. Sivakumar, K. Y. J. Song, and Y. M. Wong, "Key factors in Cu wire bonding reliability: remnant aluminum and Cu/Al IMC thickness," in *Electronics Packaging Technology Conference, 2008. EPTC 2008. 10th*, 2008, pp. 971–975.

128. C. J. Hang, C. Q. Wang, M. Mayer, Y. H. Tian, Y. Zhou, and H. H. Wang, "Growth behavior of Cu/Al intermetallic compounds and cracks in copper ball bonds during isothermal aging," *Microelectronics Reliability*, vol. 48, pp. 416–424, 2008.
129. R. Pelzer, M. Nelhiebel, R. Zink, S. Wöhlert, A. Lassnig, and G. Khatibi, "High temperature storage reliability investigation of the Al–Cu wire bond interface," *Microelectronics Reliability*.
130. H. Xu, V. L. Acuff, C. Liu, V. V. Silberschmidt, and Z. Chen, "Facilitating intermetallic formation in wire bonding by applying a pre-ultrasonic energy," *Microelectronic Engineering*, vol. 88, pp. 3155–3157, Oct 2011.
131. H. Xu, C. Liu, V. V. Silberschmidt, Z. Chen, J. Wei, and M. Sivakumar, "Effect of bonding duration and substrate temperature in copper ball bonding on aluminium pads: a TEM study of interfacial evolution," *Microelectronics Reliability*, vol. 51, pp. 113–118, Jan 2011.
132. Y. H. Tian, I. Lum, S. J. Won, S. H. Park, J. P. Jung, M. Mayer, and Y. Zhou, "Experimental study of ultrasonic wedge bonding with copper wire," in *Electronic Packaging Technology, 2005 6th International Conference on*, 2005, pp. 389–393.
133. Y.-h. Tian, C.-q. Wang, and Y. N. Zhou, "Bonding mechanism of ultrasonic wedge bonding of copper wire on Au/Ni/Cu substrate," *Transactions of Nonferrous Metals Society of China*, vol. 18, pp. 132–137, 2008.
134. S. Thomas and D. Reynoso, "Reliability of Cu wire bonding on active area for automotive applications," in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 363–368.
135. D. Degryse, B. Vandeveldel, and E. Beyne, "FEM study of deformation and stresses in copper wire bonds on Cu low-k structures during processing," in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, pp. 906–912 Vol.1.
136. C. Jian, D. Degryse, P. Ratchev, and I. De Wolf, "Mechanical issues of Cu-to-Cu wire bonding," *Components and Packaging Technologies, IEEE Transactions on*, vol. 27, pp. 539–545, 2004.
137. C.-L. Yeh, Y.-S. Lai, and J.-D. Wu, "Dynamic analysis of wirebonding process on Cu/low-k wafers," in *Electronics Packaging Technology, 2003 5th Conference (EPTC 2003)*, 2003, pp. 282–286.
138. X. Gu, J. Antol, Y. F. Yao, and K. H. Chua, "A reliable wire bonding on 130 nm Cu/low-k device," in *Electronics Packaging Technology, 2003 5th Conference (EPTC 2003)*, 2003, pp. 707–711.
139. C.-L. Chuang, J.-N. Aoh, and R.-F. Din, "Oxidation of copper pads and its influence on the quality of Au/Cu bonds during thermosonic wire bonding process," *Microelectronics Reliability*, vol. 46, pp. 449–458, 2006.
140. J.-N. Aoh and C.-L. Chuang, "Development of a thermosonic wire-bonding process for gold wire bonding to copper pads using argon shielding," *Journal of Electronic Materials*, vol. 33, pp. 300–311, 2004.
141. Y. S. Zheng, Y. J. Su, B. Yu, and P. D. Foo, "Investigation of defect on copper bond pad surface in copper/low k process integration," *Microelectronics Reliability*, vol. 43, pp. 1311–1316, 2003.
142. M. Sivakumar, V. Kripesh, C. Ser Choong, C. Tai Chong, and L. Aik Lim, "Reliability of wire bonding on low-k dielectric material in damascene copper integrated circuits PBGA assembly," *Microelectronics Reliability*, vol. 42, pp. 1535–1540, 2002.
143. C. N. B. Poh, V. Tee Heng, L. Tham Veng, and E. N. C. Chye, "Process development of 17.5 μm gold wire bonding on C65 low-k devices with probe marks," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 359–363.
144. S. Chungpaiboonpatana and F. G. Shi, "Packaging of copper/low-k IC devices: a novel direct fine pitch gold wirebond ball interconnects onto copper/low-k terminal pads," *Advanced Packaging, IEEE Transactions on*, vol. 27, pp. 476–489, 2004.

145. M.-c. Han, B.-y. Yan, J. Z. Yao, T. A. Tran, S. Lee, and J. Li, "Low-k CMOS65 ball grid array 47 um pitch wire bonding process development," in *Electronics Packaging Technology Conference, 2007. EPTC 2007. 9th*, 2007, pp. 613–617.
146. V. Kripesh, M. Sivakumar, L. Loon Aik, R. Kumar, and M. K. Iyer, "Wire bonding process impact on low-k dielectric material in damascene copper integrated circuits," in *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*, 2002, pp. 873–880.
147. P.-C. Chin, C.-Y. Hu, H.-C. Hsu, S.-L. Fu, C.-L. Yeh, and Y.-S. Lai, "Characteristic of heat affected zone in thin gold wire and dynamic transient analysis of wire bonding for micro-structure of Cu/Low-k wafer," in *Microsystems, Packaging, Assembly and Circuits Technology, 2007. IMPACT 2007. International*, 2007, pp. 297–300.
148. C.-L. Yeh and Y.-S. Lai, "Comprehensive dynamic analysis of wirebonding on Cu/low-k wafers," *Advanced Packaging, IEEE Transactions on*, vol. 29, pp. 264–270, 2006.
149. H.-C. Hsu, W.-Y. Chang, S.-L. Fu, C.-L. Yeh, and Y.-S. Lai, "Dynamic finite element analysis on underlay microstructure of Cu/low-k wafer during bonding process," in *Electronic Materials and Packaging, 2007. EMAP 2007. International Conference on*, 2007, pp. 1–6.
150. W. Huang, "Computational modeling and optimization for wire bonding process on Cu/low-k wafers," in *Electronic Packaging Technology & High Density Packaging, 2009. ICEPT-HDP '09. International Conference on*, 2009, pp. 344–352.
151. X. Fan, K. Qian, T. Wang, Y. Cong, M. Zhao, B. Zhang, and J. Wang, "Nanoindentation investigation of copper bonding wire and ball," in *Electronic Packaging Technology & High Density Packaging, 2009. ICEPT-HDP '09. International Conference on*, 2009, pp. 790–794.
152. S. Murali, N. Srikanth, and C. J. Vath III, "An analysis of intermetallics formation of gold and copper ball bonding on thermal aging," *Materials Research Bulletin*, vol. 38, pp. 637–646, 2003.
153. M. H. M. Kouters, G. H. M. Gubbels, and C. A. Yuan, "Characterization of intermetallic compounds in Cu-Al ball bonds: mechanical properties, delamination strength and thermal conductivity," in *Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 2012 13th International Conference on*, 2012, pp. 1/9–9/9.
154. P. Ratchev, S. Stoukatch, and B. Swinnen, "Mechanical reliability of Au and Cu wire bonds to Al, Ni/Au and Ni/Pd/Au capped Cu bond pads," *Microelectronics Reliability*, vol. 46, pp. 1315–1325, 2006.
155. H. Xu, C. Liu, and V. Silberschmidt, "Effect of thermal aging on interfacial behaviour of copper ball bonds," in *Electronics System-Integration Technology Conference, 2008. ESTC 2008. 2nd*, 2008, pp. 891–896.
156. S. Lee, T. Uehling, and H. L. III., "Freescale copper wire - analysis, results and implementation," 2012.
157. S. H. Kim, J. W. Park, S. J. Hong, and J. T. Moon, "The interface behavior of the Cu-Al bond system in high humidity conditions," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 545–549.
158. H. Xu, C. Liu, V. V. Silberschmidt, S. S. Pramana, T. J. White, Z. Chen, and V. L. Acoff, "New mechanisms of void growth in Au-Al wire bonds: volumetric shrinkage and intermetallic oxidation," *Scripta Materialia*, vol. 65, pp. 642–645, 2011.
159. Y. Y. Tan and F. K. Yong, "Cu-Al IMC micro structure study in Cu wire bonding with TEM," in *Physical and Failure Analysis of Integrated Circuits (IPFA), 2010 17th IEEE International Symposium on the*, 2010, pp. 1–4.
160. H. Xu, C. Liu, V. V. Silberschmidt, S. S. Pramana, T. J. White, Z. Chen, and V. L. Acoff, "Intermetallic phase transformations in Au-Al wire bonds," *Intermetallics*, vol. 19, pp. 1808–1816, 2011.
161. L. S. Yeoh, "Characterization of intermetallic growth for gold bonding and copper bonding on aluminum metallization in power transistors," in *Electronics Packaging Technology Conference, 2007. EPTC 2007. 9th*, 2007, pp. 731–736.
162. Y. Funamizu and K. Watanabe, "Interdiffusion in the Al-Cu system," *Transactions of the Japan Institute of Metals*, vol. 12, pp. 147–152, 1971.

163. P. M. Hall and J. M. Morabito, "Diffusion problems in microelectronic packaging," *Thin Solid Films*, vol. 53, pp. 175–182, 1978.
164. M. Pinnel and J. Bennett, "On the formation of the ordered phases CuAu and Cu₃Au at a copper/gold planar interface," *Metallurgical and Materials Transactions A*, vol. 10, pp. 741–747, 1979.
165. Department of Defense, "MIL-STD 883G test method standard microcircuits," 2006.
166. M. S. Ramelow, "Wire bonding quality assurance and testing methods."
167. D. T. Rooney, D. P. Nager, D. Geiger, and D. Shangguan, "Evaluation of wire bonding performance, process conditions, and metallurgical integrity of chip on board wire bonds," *Microelectronics Reliability*, vol. 45, pp. 379–390, Feb 2005.
168. C. Wang, and R. Sun, "The Quality Test of Wire Bonding," *Modern Applied Science*, vol. 3, p. 7, 2009.
169. M.-C. Wang, Z.-Y. Hsieh, K.-S. Huang, C.-H. Liu, and C.-R. Lin, "Analysis of promising copper wire bonding in assembly consideration," in *Microsystems, Packaging, Assembly and Circuits Technology Conference, 2009. IMPACT 2009. 4th International*, 2009, pp. 108–111.
170. B. K. Appelt, A. Tseng, L. Yi-Shao, and C. Chun-Hsiung, "Copper wire bonding - a maturing technology," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 479–483.
171. V. Dixit, H. Davis, and M. Clark, "Wire bonding considerations-design tips for performance and reliability," *Advanced Packaging*, vol. 15, p. 6, 2006.
172. M. T. Labs, "Wire bonding semiconductor packaging."
173. J. S. S. T. Association, "Failure mechanisms and models for semiconductor devices," in *JEP122C*, ed, 2006.
174. T. N. E. P. Guideline, "Chapter A: wire bonding, level 2; conclusions and guidelines."
175. N. J. Noolu, N. M. Murdeshwar, K. J. Ely, J. C. Lippold, and W. A. Baeslack, "Degradation and failure mechanisms in thermally exposed Au-Al ball bonds," *Journal of Materials Research*, vol. 19, pp. 1374–1386, May 2004.
176. A. Teverovsky, "Effect of vacuum on high-temperature degradation of gold/aluminum wire bonds in PEMs," in *Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International*, 2004, pp. 547–556.
177. C. J. Vath, M. Gunasekaran, and R. Malliah, "Factors affecting the long term stability of Cu / Al ball bonds subjected to standard and extended HTS," in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 374–380.
178. Y. H. Lu, Y. W. Wang, B. K. Appelt, Y. S. Lai, and C. R. Kao, "Growth of CuAl intermetallic compounds in Cu and Cu(Pd) wire bonding," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1481–1488.
179. M. N. M. Ching and K. J. Lee, "Influence of nitrogen and forming gas towards palladium coated copper wire," in *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*, 2011, pp. 318–323.
180. L. Yap Siew and W. Juergen, "Characterization of palladium coated copper wire prior physical bonding assessment," in *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*, 2011, pp. 313–317.
181. T. C. Wei and A. R. Daud, "The effects of aged Cu-Al intermetallics to electrical resistance in microelectronics packaging," *Microelectronics International*, vol. 19, pp. 38–43, 2002.
182. J. Onuki, M. Koizumi, and I. Araki, "Investigation of the reliability of copper ball bonds to aluminum electrodes," *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on*, vol. 10, pp. 550–555, 1987.
183. H. J. Kim, J. Y. Lee, K. W. Paik, K. W. Koh, J. H. Won, S. H. Choi, J. Lee, J. T. Moon, and Y. J. Park, "Effects of Cu/Al intermetallic compound (IMC) on copper wire and aluminum pad bondability," in *Electronic Materials and Packaging, 2001. EMAP 2001. Advances in*, 2001, pp. 44–51.

184. C. L. Gan, E. Ng, B. Chan, F. Classe, T. Kwuanjai, and U. Hashim, "Wearout Reliability and Intermetallic Compound Diffusion Kinetics of Au and PdCu Wires Used in Nanoscale Device Packaging," *Journal of Nanomaterials*, vol. 2013, 2013.
185. S. Na, T. Hwang, J. Park, J. Kim, H. Yoo, and C. Lee, "Characterization of Intermetallic Compound (IMC) growth in Cu wire ball bonding on Al pad metallization," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1740–1745.
186. D. Solutions, "Predicting reliability of first-level wire bonds," ed.
187. M. Pecht, *Product reliability, maintainability, and supportability handbook*: CRC Press, 2010.
188. J. M. Hu, M. Pecht, and A. Dasgupta, "A probabilistic approach for predicting thermal fatigue life of wire bonding in microelectronics," *Journal of Electronic Packaging*, vol. 113, p. 275, 1991.
189. C. Gan and U. Hashim, "Reliability assessment and mechanical characterization of Cu and Au ball bonds in BGA package," *Journal of Materials Science: Materials in Electronics*, pp. 1–9.
190. C. E. Tan, "Copper wire bonding process in leaded packages with zero loss in quality, capacity, scrap & machine efficiency," in *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*, 2011, pp. 324–328.
191. H. Liu, Z. Zhao, Q. Chen, J. Zhou, M. Du, S. Kim, J. Chae, and M. Chung, "Reliability of copper wire bonding in humidity environment," in *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*, 2011, pp. 53–58.
192. C. Gan, E. Ng, B. Chan, U. Hashim, and F. Classe, "Technical barriers and development of Cu wirebonding in nanoelectronics device packaging," *Journal of Nanomaterials*, vol. 2012, p. 96, 2012.
193. C. W. Tan, A. R. Daud, and M. A. Yarmo, "Corrosion study at Cu–Al interface in microelectronics packaging," *Applied Surface Science*, vol. 191, pp. 67–73, 2002.
194. T. Uno and T. Yamada, "Improving humidity bond reliability of copper bonding wires," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 1725–1732.
195. H. Abe, D. C. Kang, T. Yamamoto, T. Yagihashi, Y. Endo, H. Saito, T. Horie, H. Tamate, Y. Ejiri, and N. Watanabe, "Cu wire and Pd-Cu wire package reliability and molding compounds," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 1117–1123.
196. R. Lawson, "A review of the status of plastic encapsulated semiconductor component reliability," *British Telecom technology journal*, vol. 2, pp. 95–111, 1984.
197. D. S. Peck, "Comprehensive model for humidity testing correlation," in *Reliability Physics Symposium, 1986. 24th Annual*, 1986, pp. 44–50.
198. A. Teverovsky, "NASA Electronic Parts and Packaging Program (NEPP)," 2005.
199. J. R. Black, "Electromigration failure modes in aluminum metallization for semiconductor devices," *Proceedings of the IEEE*, vol. 57, pp. 1587–1594, 1969.
200. C. Breach, "The great debate: copper vs. gold ball bonding."
201. H. T. Orchard and A. L. Greer, "Electromigration effects on intermetallic growth at wire-bond interfaces," *Journal of Electronic Materials*, vol. 35, pp. 1961–1968, Nov 2006.
202. E. Zin, N. Michael, S. H. Kang, K. H. Oh, U. Chul, J. S. Cho, J. T. Moon, and C. U. Kim, "Mechanism of electromigration in Au/Al wirebond and its effects," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 943–947.
203. S. Horowitz and I. Blech, "Electromigration in Al/Cu/Al films observed by transmission electron microscopy," *Materials Science and Engineering*, vol. 10, pp. 169–174, 1972.
204. N. Bertolino, J. Garay, U. Anselmi-Tamburini, and Z. Munir, "High-flux current effects in interfacial reactions in Au–Al multilayers," *Philosophical Magazine B*, vol. 82, pp. 969–985, 2002.
205. C.-K. Hu, "Electromigration failure mechanisms in bamboo-grained Al (Cu) interconnections," *Thin Solid Films*, vol. 260, pp. 124–134, 1995.

206. J. Tao, N. W. Cheung, and C. Hu, "Electromigration characteristics of copper interconnects," *Electron Device Letters, IEEE*, vol. 14, pp. 249–251, 1993.
207. L. Arnaud, G. Tartavel, T. Berger, D. Mariolle, Y. Gobil, and I. Touet, "Microstructure and electromigration in copper damascene lines," *Microelectronics Reliability*, vol. 40, pp. 77–86, 2000.
208. C. D. Breach and R. Holliday, "Factors affecting reliability of gold and copper in ball bonding," in *Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), 2010 11th International Conference on*, 2010, pp. 446–451.
209. A. Shah, M. Mayer, Y. N. Zhou, S. J. Hong, and J. T. Moon, "Low-stress thermosonic copper ball bonding," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 32, pp. 176–184, 2009.
210. M. C. Han, B. Y. Yan, H. Y. Zhang, J. Z. Yao, and J. Li, "Low K CMOS65 ball grid array 40 μm pitch wire bonding process development," in *Electronics Packaging Technology Conference, 2008. EPTC 2008. 10th*, 2008, pp. 457–462.
211. D. Degryse, B. Vandevelde, and E. Beyne, "Mechanical FEM simulation of bonding process on Cu low-k wafers," *Components and Packaging Technologies, IEEE Transactions on*, vol. 27, pp. 643–650, 2004.
212. C. C. Lee, T. A. Tran, and Y. K. Au, "Metal lift failure modes during fine pitch wire bonding low-k devices with bond over active (BOA) design," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 31–36.
213. C.-F. Yu, C.-M. Chan, L.-C. Chan, and K.-C. Hsieh, "Cu wire bond microstructure analysis and failure mechanism," *Microelectronics Reliability*, vol. 51, pp. 119–124, 2011.
214. X. Zhang, X. Lin, and Y. Chen, "The reliability evaluation of Cu wire bonding by using focus ion beam system," in *Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), 2010 11th International Conference on*, 2010, pp. 1049–1052.
215. C. K. J. Teo, "17.5 μm thin Cu wire bonding for fragile low-k wafer technology," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 355–358.
216. L. C. Chian, N. K. Chai, L. C. Chia, C. M. King, L. O. Seng, and C. K. Yau, "Copper wire reliability and bonding integrity robustness on cratering sensitive bond pad structure," in *Electronics Manufacturing and Technology, 31st International Conference on*, 2006, pp. 354–364.
217. B. Chylak, J. Ling, H. Clauberg, and T. Thieme, "Next generation nickel-based bond pads enable copper wire bonding," *ECS Transactions*, vol. 18, pp. 775–785, 2009.
218. A. Shah, M. Mayer, Y. Zhou, J. Persic, and J. T. Moon, "Optimization of ultrasound and bond force to reduce pad stress in thermosonic Cu ball bonding," in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 10–15.
219. L. England, S. T. Eng, C. Liew, and H. H. Lim, "Cu wire bond parameter optimization on various bond pad metallization and barrier layer material schemes," *Microelectronics Reliability*, vol. 51, pp. 81–87, 2011.
220. Q. Chen, Z. Zhao, H. Liu, J. Chae, S. Kim, and M. Chung, "Investigation of various pad structure influence for copper wire bondability," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*, 2011, pp. 419–422.
221. G. G. Harman and C. E. Johnson, "Wire bonding to advanced copper, low-k integrated circuits, the metal/dielectric stacks, and materials considerations," *Components and Packaging Technologies, IEEE Transactions on*, vol. 25, pp. 677–683, 2002.
222. G. V. Periasamy, V. Kripesh, C.-H. Tung, and L. Loon Aik, "Wire bonding on a novel immersion gold capped copper metallized integrated circuit," in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, pp. 358–364 Vol.1.
223. H. C. Hsu, H.-S. Chang, S.-C. Tsao, and S. L. Fu, "Advanced finite element model on copper wire ball bonding," in *Electronic Manufacturing Technology Symposium (IEMT), 2010 34th IEEE/CPMT International*, 2010, pp. 1–6.
224. M. Sekihara and T. Okita, "Ultrasonic wire bonding method for a semiconductor device," 2012.

225. T. A. Tran, L. Yong, B. Williams, S. Chen, and A. Chen, "Fine pitch probing and wirebonding and reliability of aluminum capped copper bond pads," in *Electronic Components & Technology Conference, 2000. 2000 Proceedings. 50th*, 2000, pp. 1674–1680.
226. M. Ozkok, Robert, H. and Clauberg, H. "Copper wire bonding on pure palladium surface finishes - eliminating the gold cost from the electronic packaging", in *Journal of Surface Mount Technology*, vol. 24, no.2.
227. K. Johal, H. Robert, K. Desa, Q.H. Low and R. Huemoeller, "Performance and reliability evaluation of alternative surface finishes for wire bond and flip chip BGA applications." *Pan Pacific Symposium Conference Proceedings*, 2006.
228. R. W. Johnson, M. J. Palmer, M. J. Bozack, and T. Isaacs-Smith, "Thermosonic gold wire bonding to laminate substrates with palladium surface finishes," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 22, pp. 7–15, 1999.
229. W. H. Li, A. Acuesta, M. G. Mercado, N. T. Malonzo, and R. S. Cabral, "Cu wire bonding in Ni/Pd/Au-Ag and roughened Ni/Pd/Au-Ag pre-plated leadframe packages," in *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*, 2011, pp. 794–797.
230. M. Özkök, M. Gensicke, G. Heinz, H. Roberts, and J. McGurran, "Resistance of common PWB Surface Finishes against Corrosion in Harsh Environments," in *SMTA International Conference*, p. 9, 2010.
231. E. P. Leng, P. Z. Song, A. Y. Kheng, C. C. Yong, T. T. Anh, J. Arthur, H. Downey, V. Mathew, and C. Y. Yin, "High temperature automotive application: a study on fine pitch Au and Cu WB integrity vs. Ni thickness of Ni/Pd/Au bond pad on C90 low k wafer technology," in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 349–354.
232. G. Khatibi, S. Puchner, B. Weiss, A. Zechmann, T. Detzel, and H. Hutter, "Influence of titanium surface contamination on the reliability of Al wire bonds," in *Microelectronics and Packaging Conference (EMPC), 2011 18th European*, 2011, pp. 1–7.
233. P. Yu, J. Su, G. Qiang, L. Ming, and N. Chornig, "Study of aluminum pad contamination sources during wafer fabrication, shipping, storage and assembly," in *High Density packaging and Microsystem Integration, 2007. HDP '07. International Symposium on*, 2007, pp. 1–3.
234. S. Alberici, D. Coulon, P. Joubin, Y. Mignot, L. Oggioni, P. Petruzza, D. Piumi, and L. Zanotti, "Surface treatment of wire bonding metal pads," *Microelectronic Engineering*, vol. 70, pp. 558–565, 2003.
235. K. H. Ernst, D. Grman, R. Hauert, and E. Holländer, "Fluorine-induced corrosion of aluminum microchip bond pads: an XPS and AES analysis," *Surface and Interface Analysis*, vol. 21, pp. 691–696, 1994.
236. M. Petzold, L. Berthold, D. Katzer, H. Knoll, D. Memhard, P. Meier, and K. D. Lang, "Surface oxide films on aluminum bondpads: influence on thermosonic wire bonding behavior and hardness," *Microelectronics Reliability*, vol. 40, pp. 1515–1520, 2000.
237. S. Puchner, Zechmann, A., Detzel, T., Hutter, H. "Titanium layers on aluminum bond pads: characterization of thin layers on rough substrates," *Surface and Interface Analysis*, vol. 42, p. 4, 2010.
238. T. Y. Lin, W. S. Leong, K. H. Chua, R. Oh, Y. Miao, J. S. Pan, and J. W. Chai, "The impact of copper contamination on the quality of the second wire bonding process using X-ray photoelectron spectroscopy method," *Microelectronics Reliability*, vol. 42, pp. 375–380, 2002.
239. Y. Huang, Kim, H. J., McCracken, M., Viswanathan, G., Pon, F., Mayer, M., Zhou, Y.N., "Effect of Pd surface roughness on the bonding process and high temperature reliability of Au ball bonds," *Journal of Electronic Materials*, vol. 40, p. 8, 2011.
240. D. T. Rooney, D. Nager, D. Geiger, and D. Shangguan, "Evaluation of wire bonding performance, process conditions, and metallurgical integrity of chip on board wire bonds," *Microelectronics Reliability*, vol. 45, pp. 379–390, 2005.
241. J. Li, Z. Zhao, and L. Jaisung, "Wire bonding performance and solder joint reliability investigation on ENEPIG finish substrate," in *Electronic Packaging Technology & High*

- Density Packaging (ICEPT-HDP), 2010 11th International Conference on*, 2010, pp. 240–245.
242. K. W. Lam, H.-M. Ho, S. Stoukatch, M. Van De Peer, P. Ratchev, C. J. Vath, A. Schervan, and E. Beyne, “Fine pitch copper wire bonding on copper bond pad process optimization,” in *Electronic Materials and Packaging, 2002. Proceedings of the 4th International Symposium on*, 2002, pp. 63–68.
 243. P. Banda, H.-M. Ho, C. Whelan, W. Lam, C. J. Vath, and E. Beyne, “Direct Au and Cu wire bonding on Cu/low-k BEOL,” in *Electronics Packaging Technology Conference, 2002. 4th*, 2002, pp. 344–349.
 244. J. D. Getty, “How plasma-enhanced surface modification improves the production of micro-electronics and optoelectronics,” *Chip scale review*, p. 4, 2002.
 245. Y. H. Chan, J. K. Kim, D. Liu, P. C. K. Liu, Y. M. Cheung, and M. W. Ng, “Effect of plasma treatment of Au-Ni-Cu bond pads on process windows of Au wire bonding,” *Advanced Packaging, IEEE Transactions on*, vol. 28, pp. 674–684, 2005.
 246. B. Chylak, “Developments in fine pitch copper wire bonding production,” in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 1–6.
 247. T. P. Chai, J. Tan, M. Sivakumar, J. Premkumar, J. Song, and Y. M. Wong, “Super heavy 6.0 mils Cu wire ball bonding,” in *Electronic Manufacturing Technology Symposium (IEMT), 2008 33rd IEEE/CPMT International*, 2008, pp. 1–5.
 248. S. Schindler, M. Wohnig, and K. J. Wolter, “Fine pitch Cu wire bond process for integrated circuit devices for high volume production,” in *Electronics System-Integration Technology Conference, 2008. ESTC 2008. 2nd*, 2008, pp. 767–770.
 249. E. P. Leng, C. T. Siong, L. B. Seong, P. Leong, Gunasekaran, J. Song, K. S. Mock, C. W. Siew, S. Sivakumar, B. K. Wong, and C. Weily, “Ultra fine pitch Cu wire bonding on C45 ultra low k wafer technology,” in *Electronics Packaging Technology Conference (EPTC), 2010 12th*, 2010, pp. 484–488.
 250. M. R. Ibrahim, C. C. Yong, L. Lim, J. Lu, T. P. Low, and C. A. Poh, “The challenges of fine pitch copper wire bonding in BGA packages,” in *Electronics Manufacturing and Technology, 31st International Conference on*, 2006, pp. 347–353.
 251. B. K. Appelt, A. Tseng, and L. Yi-Shao, “Fine pitch copper wire bonding-why now?,” in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 469–472.
 252. S. Schindler, M. Wohnig, and K. J. Wolter, “Development of a fine pitch copper wire bond process for integrated circuit devices,” in *Electronics Technology, 2008. ISSE '08. 31st International Spring Seminar on*, 2008, pp. 385–388.
 253. L. T. Nguyen, D. McDonald, A. R. Danker, and P. Ng, “Optimization of copper wire bonding on Al-Cu metallization,” *Components, Packaging, and Manufacturing Technology, Part A, IEEE Transactions on*, vol. 18, pp. 423–429, 1995.
 254. C. A. Palesko and E. J. Vardaman, “Cost comparison for flip chip, gold wire bond, and copper wire bond packaging,” in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, 2010, pp. 10–13.
 255. J. F. J. M. Caers, A. Bischoff, J. Falk, and J. Roggen, “Conditions for reliable ball-wedge copper wire bonding,” in *Electronic Manufacturing Technology Symposium, 1993., Proceedings of 1993 Japan International*, 1993, pp. 312–315.
 256. V. P. Ganesh and M. Sivakumar, “Process development for ultra low loop reverse wire bonding on copper bond pad metallization,” in *Electronics Packaging Technology Conference, 2002. 4th*, 2002, pp. 356–360.
 257. T. Saraswati, E. P. P. Theint, D. Stephan, H. M. Goh, E. Pasamanero, D. R. M. Calpito, F. W. Wulff, and C. D. Breach, “High temperature storage (HTS) performance of copper ball bonding wires,” in *Electronic Packaging Technology Conference, 2005. EPTC 2005. Proceedings of 7th*, 2005, p. 6 pp.
 258. C. Yi Heang, H. Meiyang, and C. E. Tseng, “The properties comparison between Au and Cu wires bond in DRAM component,” in *Physical and Failure Analysis of Integrated Circuits (IPFA), 2011 18th IEEE International Symposium on the*, 2011, pp. 1–4.

259. B. S. Kumar, M. Sivakumar, W. Chua Choon, M. Li, Y. Keng, and J. Song, "Cu wire bonding with Cu BSOB for SiP & stacked die application: challenges & solutions," in *Electronics Packaging Technology Conference, 2009. EPTC '09. 11th*, 2009, pp. 16–20.
260. C. L. Yen, Y. C. Lee, and Y. S. Lai, "Vibration and bondability analysis of fine-pitch Cu wire bonding," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*, 2011, pp. 1–7.
261. H. Liu, Z. Zhao, Q. Chen, J. Zhou, M. Du, S. Kim, J. Chae, and M. Chung, "Reliability of copper wire bonding in humidity environment," in *Electronics Packaging Technology Conference (EPTC), 2011 IEEE 13th*, 2011, pp. 53–58.
262. H. Seki, P. Chen, H. Nakatake, S. i. Zenbutsu, and S. Itoh, "Study of EMC for Cu bonding wire application," in *CPMT Symposium Japan, 2010 IEEE*, 2010, pp. 1–3.
263. C. L. Gan, T. T. Toong, C. P. Lim, and C. Y. Ng, "Environmental friendly package development by using copper wirebonding," in *Electronic Manufacturing Technology Symposium (IEMT), 2010 34th IEEE/CPMT International*, 2010, pp. 1–5.
264. J. Brunner, I. Wei Qin, and B. Chylak, "Advanced wire bond looping technology for emerging packages," in *Electronics Manufacturing Technology Symposium, 2004. IEEE/CPMT/SEMI 29th International*, 2004, pp. 85–90.
265. F. Lee Kuan, O. Kwon, O. Yauw, D. Capistrano, and B. Milton, "Ultra low loop conversion from gold to copper wire," in *Electronic Manufacturing Technology Symposium (IEMT), 2010 34th IEEE/CPMT International*, 2010, pp. 1–5.
266. G. O'Malley, P. Su, H. Fu, M. Bayes, and M. Tsuriya, "Current industry adoption of fine-pitch Cu wire bonding and investigation focus at iNEMI," in *Microelectronics and Packaging Conference (EMPC), 2011 18th European*, 2011, pp. 1–4.
267. H. Abe, D. C. Kang, T. Yamamoto, T. Yagihashi, Y. Endo, H. Saito, T. Horie, H. Tamate, Y. Ejiri, N. Watanabe, and T. Iwasaki, "Cu wire and Pd-Cu wire package reliability and molding compounds," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 1117–1123.
268. S. Murali and N. Srikanth, "Acid decapsulation of epoxy molded IC packages with copper wire bonds," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 29, pp. 179–183, 2006.
269. J. Tang, J. Schelen, and C. Beenakker, "Flexible system for real-time plasma decapsulation of copper wire bonded IC packages," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 1764–1769.
270. J. Tang, H. Ye, J. B. J. Schelen, and C. I. M. Beenakker, "Plasma decapsulation of plastic IC packages with copper wire bonds for failure analysis," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*, 2011, pp. 1–5.
271. J. Tang, E. Reinders, C. Revenberg, J. Schelen, and C. Beenakker, "Decapsulation of high pin count IC packages with palladium coated copper wire bonds using an atmospheric pressure plasma," in *Electronic Packaging Technology Conference*, Singapore, 2012.
272. S. ChipPAC. (2011). *Copper wirebond*. Available: http://www.statschippac.com/news/newscenter/2011/~media/Files/Package%20Datasheets/Cu_wb.ashx

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